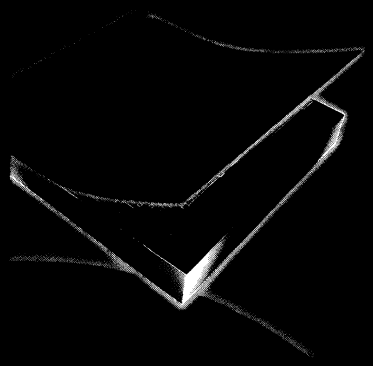
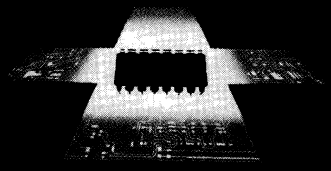
IC DATA BOOK





CSC™ CHERRY SEMICONDUCTOR

Cherry Semiconductor Corporation makes no representation that the use of any circuitry described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

CSC™ reserves the right to make changes to the products contained in this data book to improve performance, reliability, or manufacturability. Consequently, contact CSC™ for the latest available specifications and performance data.

LIFE SUPPORT POLICY

CSC™'s products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Cherry Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is a component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Note: Information in this data book is believed to be accurate and reliable, no responsibility is assumed by Cherry Semiconductor Corporation for its use.

INTEGRATED CIRCUITS DATA BOOK

INTRODUCTION

From its inception in 1972, Cherry Semiconductor has maintained a strong commitment to excellence in the design and manufacture of bipolar integrated circuits.

Processing technologies include Linear Bipolar, I^2L Digital, Linear/I^2L combinations on the same chip, Optoelectronic Circuits, Low Power Schottky, and Flip-Chip Metallurgy.

Our modern plant has been furnished with the latest processing and production equipment, including microprocessor controlled diffusion furnaces, projection mask aligners, vertical epitaxial reactors, electron beam evaporators, sputtering systems, scanning electron microscope (SEM), and computerized testing stations. All critical processing steps are performed in a VLSI environment in Class 100 clean rooms, specially controlled for temperature and humidity, and isolated from external vibration.

CSC™ offers three basic types of IC solutions, in order to provide the system designer the optimum solution in applications utilizing linear and mixed linear/digital circuitry. The expanding CSC™ line of standard ICs is extensively used in dedicated automotive, memory management, power supply and motor control applications. Full custom ICs are developed for high-volume, long-term programs. Finally, GENESIS™ Semicustom linear and linear/digital arrays offer a wide range of user options at a fraction of the cost and leadtime of custom circuits.

Cherry Semiconductor Corporation
2000 South County Trail • East Greenwich, RI 02818
Phone: (401)885-3600 • Telex:(WUI)6817157
Telefax (401)885-5786

INDEX TO TYPE NUMBERS

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

MFR ABBREVIATION KEY

ABV	COMPANY	ABV	COMPANY
EL	Elantec	PH	Phillips
FC	Fairchild	SIG	Signetics
GP	Gennum	SG	Silicon General
HA	Harris	SGS	SGS
LT	Linear Technology	SP	Sprague
ML	Micro Linear	SSI	Silicon Systems
MOT	Motorola	TI	Texas Instruments
NS	National	UC	Unitrode
PB	Ericsson	VTC	VTC Inc.

COMPETITIVE TYPE	MFR	CSC EQUIVALENT
EHA2017	EL	CS-2017
GP605	GP	CS-3805A
LT1009	LT	CS-1009
LT1070CT	LT	CS-1070
ML117	ML	CS-117
ML510A	ML	CS-510A
MC3484	MOT	CS-288
MC34017	MOT	CS-34017
ML1819	NS	CS-189
LM2907N	NS	CS-2907N14
LM2907N8	NS	CS-2907N8
LM2917N	NS	CS-2917N14
LM2917N8	NS	CS-2917N8
LM2925	NS	CS-925
LM2935	NS	CS-935
PBL3717A	PB	CS-3717A
PBL3770	PB	CS-3770
SG2524BJ	SG	CS-2524AJ
SG2524BN	SG	CS-2524AN
SG2525AN	SG	CS-2525AN
SG2527AJ	SG	CS-2527AJ
SG2527AN	SG	CS-2527AN
SG2842J	SG	CS-2842AJ
SG2842N	SG	CS-2842AN
SG2843J	SG	CS-2843AJ
SG2843N	SG	CS-2843AN
SG3524BJ	SG	CS-3524AJ
SG3524BN	SG	CS-3524AN
SG3844J	SG	CS-3844J
L293D	SGS	CS-293D
L298	SGS	CS-298
L165	SGS	CS-365
ULN3304M	SP	CS-102
SSI32H101A	SSI	CS-101A
SSI32H116	SSI	CS-116
SSI32R117	SSI	CS-117
SSI32R510A	SSI	CS-510A
SSI32R511	SSI	CS-511
SSI32R514	SSI	CS-514
SSI32P541	SSI	CS-541
SSI32R570	SSI	CS-570

COMPETITIVE TYPE	MFR	CSC EQUIVALENT
TL493CN	TI	CS-593C
TL493CJ	TI	CS-593CJ
TL494CJ	TI	CS-594CJ
TL494CN	TI	CS-594CN
TL495CJ	TI	CS-595CJ
TL495CN	TI	CS-595CN
UC2706	UC	CS-2706
UC2842D14	UC	CS-2842AD14
UC2842D8	UC	CS-2842AD8
UC2842DW16	UC	CS-2842ADW16
UC2842J	UC	CS-2842AJ
UC2842N	UC	CS-2842AN
UC2843J	UC	CS-2843AJ
UC2843N	UC	CS-2843AN
UC2844DW16	UC	CS-2844DW16
UC2844J	UC	CS-2844J
UC2844N	UC	CS-2844N
UC2845DW16	UC	CS-2845DW16
UC2845J	UC	CS-2845J
UC2845N	UC	CS-2845N
UC3610	UC	CS-299D
UC3524J	UC	CS-3524AJ
UC3524N	UC	CS-3524AN
UC3524J	UC	CS-3524J
UC3524N	UC	CS-3524N
UC3706	UC	CS-3706
UC3770J	UC	CS-3770J
UC3770N	UC	CS-3770N
UC3842AJ	UC	CS-3842AJ
UC3842AN	UC	CS-3842AN
UC493ACJ	UC	CS-593CJ
UC493ACN	UC	CS-593CN
UC494ACJ	UC	CS-594CJ
UC494ACN	UC	CS-595CN
UC495ACJ	UC	CS-595CJ
UC495ACN	UC	CS-595CN
VM101	VTC	CS-101A
VM116	VTC	CS-116
VM117	VTC	CS-117
VM201	VTC	CS-201A

SELECTION GUIDE

Selection Guide PWM Control Circuits					Temp. Range (°C)		Max Input Voltage (V)	Max Output Current (mA)	Output Drivers		# Error Amps	Oscillator Frequency		Internal Reference Voltage		Protection Features							
Type Number	Package				-25 to +85	0 to +70			#	Totem Pole		Min (kHz)	Max (kHz)	V	%	Adj Dead Time	Soft Start	Under Voltage Lockout	Current Limiting	Double Pulse Inhibit	Volt Mode	Current Mode	Reso-nant Mode
	J	N	Pins																				
CS-320		●	16		●	●	20	200	2	HI	1	1	1000	5	2	●	●	●	●	●		●	
CS-321		●	16		●	●	20	200	2	LO	1	1	1000	5	2	●	●	●	●	●		●	
CS-322		●	8		●	●	20	200	1	HI	1	1	1000					●	●	●		●	
CS-323		●	8		●	●	20	200	1	HI	1	1	1000			●		●	●	●		●	
CS-324		●	8		●	●	20	200	1	HI	1	1	1000					●	●	●		●	
CS-325		●	8		●	●	20	200	1	HI	1	1	1000			●		●	●	●		●	
CS-360 [1]		●	16			●	20	200	2	HI	1	100	1000	5.1	±2	●	●	●	●				●
CS-593C	●	●	16			●	40	200	2		1	1	300	5	±1	●		●	●	●			
CS-594C	●	●	16			C	40	200	2		2	1	300	5	±1	●		●	SEE DATA	●			
CS-595C	●	●	18			C	>40	200	2		2	1	300	5	±1	●		●	SEE DATA	●			
CS-1070			5	TO220	●		60	5000			1	40	40						●	●		●	
CS-2844	●		8		●		30	200	1	HI	1	1	250	5	±2			●	●	●		●	
CS-2845	●		8		●		30	200	1	HI	1	1	250	5	±2			●	●	●		●	
CS-3844		●	8			●	30	200	1	HI	1	1	250	5	±2			●	●	●		●	
CS-3845		●	8			●	30	200	1	HI	1	1	250	5	±2			●	●	●		●	
CS-3524	●	●	16			●	40	100	2		2		300	5	±8				●		●		
CS-3524A	●	●	16			●	40	200	2		2	.12	500	5	±2			●	●	●	●		
CS-2842A	●	●	8		●		30	200	1	HI	1	1	500	5	±1	●		SEE DATA	●	●		●	
CS-2843A	●	●	8		●		30	200	1	HI	1	1	500	5	±1	●		SEE DATA	●	●		●	
CS-3842A	●	●	8		●		30	200	1	HI	1	1	500	5	±2	●		SEE DATA	●	●		●	
CS-3843A	●	●	8		●		30	200	1	HI	1	1	500	5	±2	●		SEE DATA	●	●		●	
CS-3805A [1]	●	●	16			●	20	200	2	LO		20	1000	5	±5	●	●	●	●	●			●
CS-2841B		●	8		●		40	200	1	HI	1	1	500	5	±2			●	●	●		●	
CS-3865		●	16			●	15.5	200	2	HI	2	1	500	5	±2			●	●	●		●	

Note 1: Resonant Mode Control IC.

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

GENESIS™ SEMICUSTOM BIPOLAR ARRAYS

TYPE NUMBER	ARRAY TYPE	DIE SIZE (Mils)	Vcc RANGE (V)	BOND PADS	I^2L GATES	I/O PORTS	DIODES	TRANSISTORS			RESISTORS		
								NPN	PNP	PWR NPN	DIFFUSED	ION IMPLANT	PINCH
1100	DIGITAL & LINEAR	98 x 124	1-12	26	64	—	—	98	41	4	339	—	8
1400	DIGITAL & LINEAR	119 x 148	1-12	40	256	18	—	UP TO 69 (ANY MIX)		—	UP TO 200		—
1500	DIGITAL & LINEAR	123 x 140	1-12	30	98	—	—	122	72	4	462	—	2
2200E	LINEAR	78 x 74	1-20	18	—	—	—	40	31	2	155	—	4
2500G	LINEAR	75 x 79	1-20	18	—	—	—	58	18	2	239	—	8
2800	*Flip-Chip* LINEAR	80 x 85	1-20	16	—	—	—	58	25	2	240	—	8
3000F	LINEAR	91 x 110	1-20	24	—	—	—	92	36	4	296	—	9
3100	(MICROPOWER) LINEAR	79 x 107	1-20	22	—	—	—	85	36	3	86	261	8
3200L	LINEAR	79 x 107	1-20	22	—	—	—	85	36	3	347	—	8
3500	(OPTO) LINEAR ARRAY	75 x 97	1-20	22	—	—	—	59	24	2	206	—	8
3600	LINEAR	98 x 115	1-20	25	—	—	—	117	52	6	482	—	12
4000M	LINEAR	96 x 147	1-20	28	—	—	—	145	56	8	576	—	16
5000	LINEAR	122 x 163	1-20	40	—	—	—	199	107	8	858	—	12
7600	(L/LS) LINEAR	98 x 118	1-15	25	—	—	10 DUAL	138	26	4	384	139	—
8000	(H.V.) LINEAR	105 x 123	1-50	23	—	—	2 ZENER 28V	60	32	2	427	—	—

PACKAGES

GENESIS CHIP	PLASTIC DIP									PLCC			SOIC			WIDE (0.3") SOIC				
	8	14	16	18	20	22	24	28	40	20	28	44	8	14	16	16	18	20	24	28
1100	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
1400	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
1500		■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
2200E	■	■	■	■	■	■				■			■	■	■	■	■	■		
2500G	■	■	■	■	■	■				■			■	■	■	■	■	■		
3000F	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
3100	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
3200	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
3600	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
4000M	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
5000		■	■	■	■	■	■	■	■	■	■	■						■	■	■
7600	■	■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■
8000		■	■	■	■	■	■	■	■	■	■	■				■	■	■	■	■

CSC's 2.0 QUALITY PROGRAM

There are no national markets or borders in the electronics industry any longer. U.S. based firms increasingly are required to design and manufacture in other areas of the world along with European and Asian companies. An integrated circuit manufacturer as Cherry Semiconductor must, therefore, be able to supply its products into any environment against any competition. The absolute foundation for doing that profitably in future years is unimpeachable quality in every aspect of the CSC organization from parts that don't fail to people who won't quit:

The 2.0 program: the total CSC commitment to never ending quality improvement.

2.0 is derived from the statistical definition of the process capability index or Cpk (see Fig. 1). A quality level with a Cpk of 1, or ±3 standard deviations about the mean, reflects a defect level of 2,699 parts per million (ppm). Product with this level of quality, incorporated into another sub-assembly or module, would produce a finished system of highly suspect reliabilty. Currently, CSC is manufacturing at a defect level of less than 100 ppm, or very nearly a Cpk of 1.33 (±4 standard deviations). This level of corporate quality has brought such quality recognition as Ford's Q1 award and Chrysler's Quality Excellence award, which has been gratifying and encouraging, but only as milestones on the way to the Corporate strategic objective of Cpk = 2.0 within three years. Thus the CSC 2.0 Program.

Relationships
Defect Levels (PPM)-Capability Indices
(Cp, Cpk)-Design specification Width

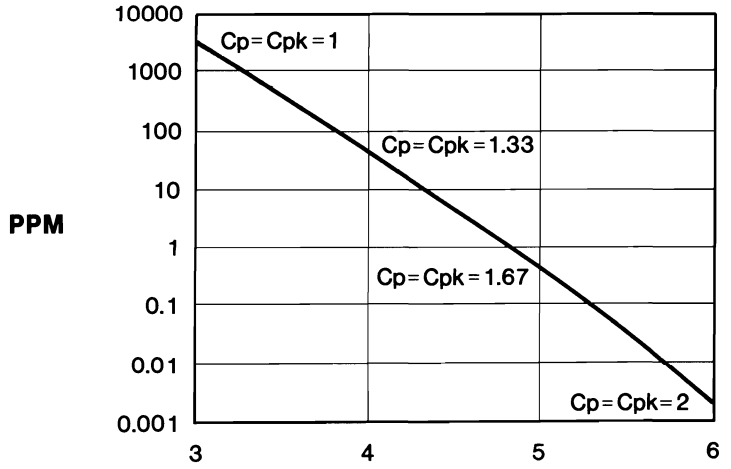


Fig. 1

A Cpk = 2.0 (±6 standard deviations) is a defect level of **two parts per billion,** or virtually zero defects. An organization with supporting facilities investment to achieve and maintain 2.0 can compete effectively and profitably anywhere in the world against anyone. To create a 2.0 environment demands a change in the operating culture normally found in Western manufacturing companies. Quality cannot be "tested" into a 2.0 product. An appreciation in each employee for the entire work that must be done must be developed, as well as on-going training to enhance the individual's performance in their own specific area of contribution, whether in finance, in circuit design, or on the manufacturing floor.

The overall direction of the 2.0 Program is set by the corporation's Quality Council, chaired by the President and made up of senior staff executives from Marketing, Finance, Manufacturing, Engineering, Facilities and Quality Assurance. During its weekly meetings, the Council reviews the program status utilizing the company's Quality Operating System which tracks performance against specific target goals. Incorporating the project-by-project approach taught by the Juran Institute and other tools, but always focusing on determining the root cause, the Council charters project teams which draw on all relevant disciplines in the company to deal with specific problem points identified from the Quality Operating System, and prioritized by their cost of quality. As each team successfully completes its function, it is disbanded and a new team chartered to work on the problem of the next lower priority.

The 2.0 Program is a clear collective statement of commitment to ever improving quality from the people of Cherry Semiconductor Corporation to their customers, vendors and to each other.

Further, more detailed, information on the CSC 2.0 Program can be obtained by contacting the office of the President, Cherry Semiconductor Corporation.

CSC™ CHERRY SEMICONDUCTOR

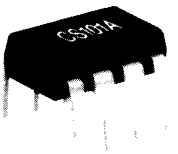
WINCHESTER SERVO PREAMP

CS-101A ™

3

DESCRIPTION

The CS-101A is a two stage differential amplifier applicable for use as a preamplifier for the magnetic servo head circuit of Winchester technology disk drives.



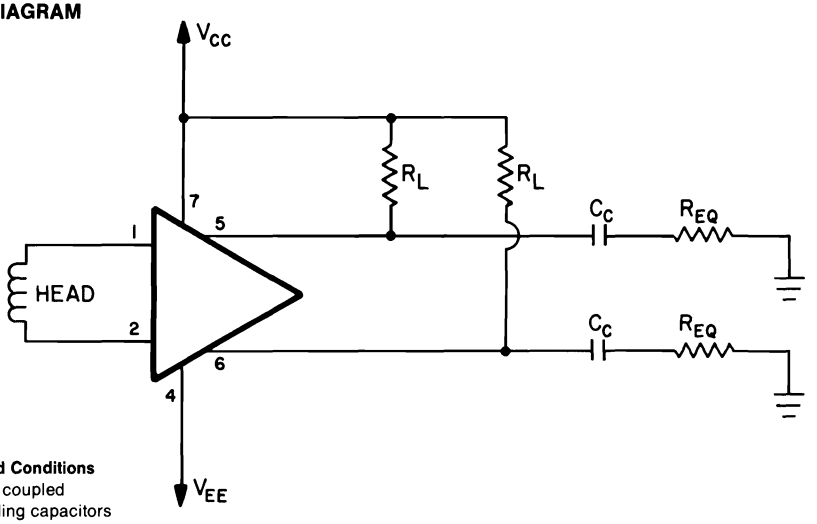
FEATURES:

- 30 MHz bandwidth
- IBM 3340 compatible performance
- Operates from any of three standard supply voltages:
  - 8.3V (IBM Compatible)
  - 10.0V
  - 12.0V
- Available in 8 pin plastic DIP and 8 pin SO

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{CC}-V_{EE})	14V
Differential Input Voltage	±1V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	0°C to 70°C

CONNECTION DIAGRAM



Recommended Load Conditions

1. Input must be AC coupled
2. C_c's are AC coupling capacitors
3. R_L's are DC bias and termination resistors, (recommended 130Ω)
4. R_{EQ} represents equivalent load resistance
5. For gain calculations $R_P = \frac{R_L \cdot R_{EQ}}{R_L + R_{EQ}}$
6. Differential gain = 0.72 R_p (±18%) (R_p in Ω)
7. Ceramic capacitors (0.1 μ F) are recommended for good power supply noise filtering

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

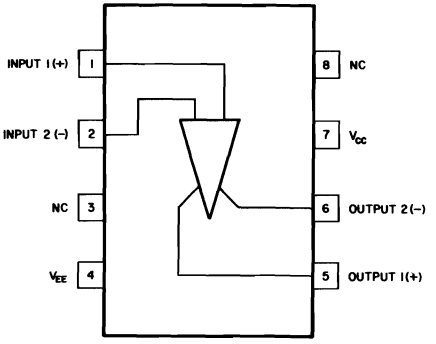
ELECTRICAL CHARACTERISTICS T_A = 25°C, (V_{CC}-V_{EE}) = 8.3V to 12V ±10%

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain (Differential)	R_p = 130Ω	77	93	110	—
Bandwidth (3dB)	Vi = 2mVpp	10	20	—	MHz
Input Resistance		800	1000	1250	Ω
Input Capacitance		—	3	—	pF
Input Dynamic Range (Differential)	R_L = 130Ω	3	—	—	mVpp
Power Supply current	(V_{CC}-V_{EE}) = 9.15V (V_{CC}-V_{EE}) = 11V (V_{CC}-V_{EE}) = 13.2V	—	26 30 35	35 40 45	mA
Output Offset (Differential)	R_s = 0, R_L = 130Ω	—	—	600	mV
Equivalent Input Noise	R_s =0, R_L = 130Ω, BW = 4MHz	—	8	14	μV
PSRR, Input Referred	R_s =0, f ≤5MHz	50	65	—	dB
Gain Sensitivity (Supply)	Δ(V_{CC}-V_{EE}) = ±10%, R_L = 130Ω	—	±1.3	—	%
Gain Sensitivity (Temp.)	T_A = 25°C to 70°C, R_L = 130Ω	—	-0.2	—	%/C
CMRR, Input Referred	f ≤5MHz	55	70	—	dB

Recommended Operating Conditions	Min.	Typ.	Max.	Units
Supply Voltage (V_{CC}-V_{EE})	7.45 9.0 10.8	8.3 10.0 12.0	9.15 11.0 13.2	V V
Input Signal Vi	—	2	—	mVpp
Ambient Temp. T_A	0	—	70	C

PIN CONNECTIONS

8 PIN PLASTIC DIP
or SO8



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-101AD	8 Lead SO
CS-101AN	8 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

WINCHESTER THIN FILM HEAD SERVO PREAMP

CS-116™

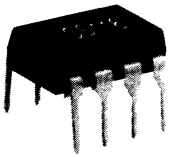
DESCRIPTION

The CS-116 is a high performance differential amplifier used as a preamplifier for the magnetic servo thin film head in Winchester disk drives.

The CS-116 is pin compatible with the CS-101A.

ABSOLUTE MAXIMUM RATINGS

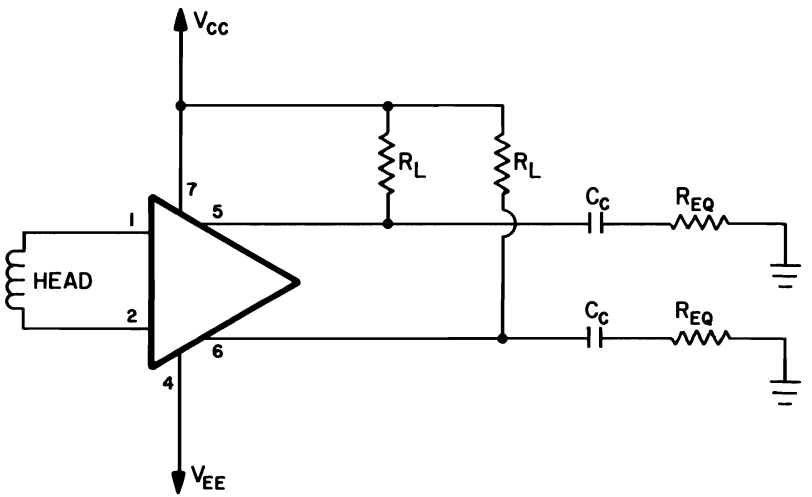
Power Supply Voltage (V_{CC}-V_{EE})	14V
Operating Power Supply Range	7.45V to 13.2V
Differential Input Voltage	± 1V
Storage Temperature Range	-65°C to 150°C
Operating Ambient Temperature	(T_A) 15°C°C to 60°C
Operating Junction Temperature	(T_J) 15°C to 125°C
Output Voltage	V_{CC}–2.0V to V_{CC} +0.4V



FEATURES:

- Low (1nV/√Hz) noise
- 50 MHz bandwidth
- IBM 3370/3380 compatible performance
- Operates from any of three standard supply voltages
  - 8.3V (IBM Compatible)
  - 10.0V
  - 12.0V
- Available in 8 pin plastic DIP and 8 pin SO

CONNECTION DIAGRAM



Recommended Load Conditions

1. Input must be AC coupled
2. C_C's are AC coupling capacitors
3. R_L's are DC bias and termination resistors, 100Ω recommended
4. R_{EQ} represents equivalent load resistance
5. Ceramic capacitors (0.1 μ F) are recommended for good power supply noise filtering

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS T_j = 15°C to 125°C, (V_{cc}-V_{EE}) = 7.9V to 13.2V, RL = 100 Ω.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain (Differential)	Vin = 1mVpp, T_A = 25°C, F = 1MHz	200	250	310	mV/mV
Bandwidth (3dB)	Vin = 1mVpp, C_L = 15pF C_L -Pin 5 to Ground -Pin 6 to Ground	20	50	—	MHz
Gain Sensitivity (Supply)	—	—	—	1.0	%/V
Gain Sensitivity (Temp.)	15°C <T_A< 55°C	—	-.0.16	—	%/C
Input Noise Voltage	Input Referred, R_S = 0	—	0.7	0.94	nV/$\sqrt{Hz}$
Input Capacitance (Differential)	Vin = 0, f = 5MHz	—	40	60	pF
Input Resistance (Differential)	—	—	200	—	Ω
Common Mode Rejection Ratio Input Referred	Vin = 100mVpp, f = 1MHz	60	70	—	dB
Input Signal Level	Common Mode	—	—	300	mVpp
Power Supply Rejection Ratio Input Referred	Vee + 100mVpp, f = 1MHz	46	52	—	dB
Input Dynamic Range (Differential)	DC input voltage where AC gain is 90% of gain with 0.2mVpp input signal	—	—	±0.75	mV
Output Offset Voltage (Differential)	Vin = 0	-600	—	600	mV
Output Voltage (Common Mode)	Inputs shorted together and Outputs shorted together	V_{CC}-1.0	V_{CC}-0.6	V_{CC}-0.45	V
Single Ended Output Resistance	RL = ∞	10	—	—	KΩ
Single Ended Output Capacitance	RL = ∞	—	—	10	pF
Power Supply current	V_{CC}-V_{EE} = 9.15V V_{CC}-V_{EE} = 11V V_{CC}-V_{EE} = 13.2V	— — —		40 42 38	mA
Input DC Voltage	Common Mode	—	V_{EE}+2.6	—	V
Input Resistance	Common Mode	—	80	—	Ω

Recommended Operating Conditions	Min.	Type	Max.	Units
Supply Voltage (VCC-VEE)	7.45 9.0 10.8	8.3 10.0 12.0	9.15 11.0 13.2	V V V
Input Signal Vin	—	1	—	mVpp
Ambient Temp. T_A	15	—	65	°C

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-116D	8 Lead SO
CS-116N	8 Lead PDIP

CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-117/117R
2, 4 or 6-Channel

WINCHESTER READ/WRITE CIRCUIT

DESCRIPTION

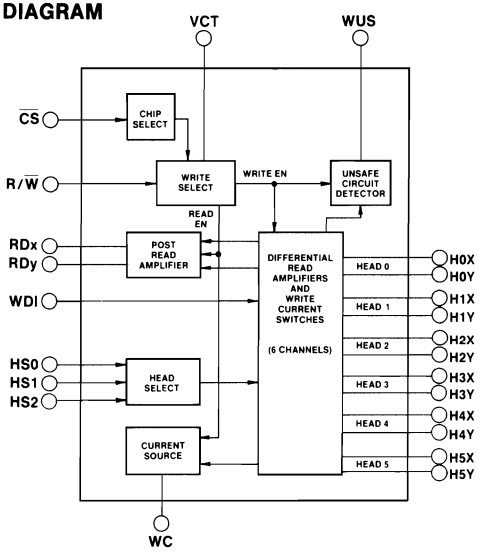
The CS-117 is a monolithic Read/Write IC designed for use in Winchester disk drive magnetic memory systems. The circuit interfaces with up to six heads to provide the necessary R/W functions, as well as control and data protect functions. LSTTL interfaces are used for the Write Data, Head Select, R/$\overline{W}$ Select, Write Unsafe, and $\overline{\text{Chip Select}}$ circuits. Write current is generated internally as a function of an external resistor. Write current transitions occur at each negative transition of the write data input. The low noise read amplifier has a typical voltage gain of 100. Balanced emitter follower outputs are used in the read amplifier. The CS-117 operates on +5V and +12V supplies.

The CS-117R performs the same function as the CS-117 with the addition of internal damping resistors.

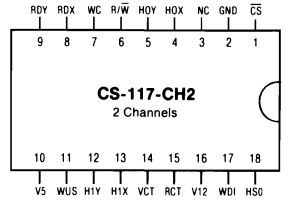
FEATURES:

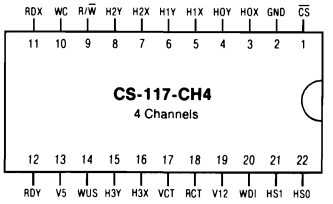
- Controls up to 6 R/W channels
- On-chip write current source, externally set
- Drives center-tapped ferrite heads
- Independent read and write busses
- TTL write data input
- LSTTL control interface
- Emitter follower read amplifier outputs
- 5V & 12V power supplies

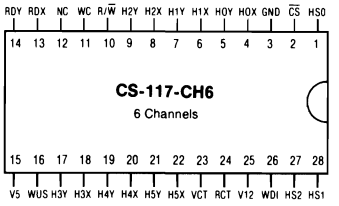
BLOCK DIAGRAM

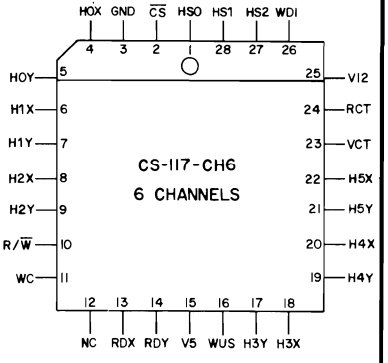


PIN CONNECTIONS









Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
(401) 885-3600 Telefax (401) 885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS: V5=4.5 to 5.5V, V12=10.8 to 13.2V, 25°C≤T_J≤125°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply				
+5V Supply Current	Read/Idle Modes	—	25	mA
+5V Supply Current	Write Mode	—	30	mA
+12V Supply Current	Read Mode	—	50	mA
+12V Supply Current	Write Mode	—	30 + IW	mA
+12V Supply Current	Idle Mode	—	25	mA
Power Dissipation	Read Mode, T_J = 125°C	—	600	mW
Power Dissipation	Write Mode, T_J = 125°C IW = 35mA, RCT = 130	—	700	mW
Power Dissipation	Write Mode, T_J = 125°C IW = 35mA, RCT = 0	—	1050	mW
Power Dissipation	Idle Mode, T_J = 125°C	—	400	mW
Logic Signals				
Input Low Voltage (VIL)		-0.3	0.8	V
Input Low Current	VIL = 0.8V	-0.4	—	mA
Input High Voltage (VIH)		2.0	V5 + 0.3	V
Input High Current	VIH = 2.0V	—	100	μA
US Low Level Voltage (VLUS)	ILUS = 8mA (Denotes Safe Condition)	—	0.5	V
US High Level Current (IHUS)	VHUS = 5.0V (Denotes unsafe condition)	—	100	μA
Write Mode Iw=25mA, Lh=10uH, Rd=750Ω, f(Data)=5MHz, CL (RDX, RDY)≤20pF				
Write Current Range		10	35	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7	—	VpK
Unselected Diff. Head Current		—	2	mApK
Differential Output Capacitance		—	15	pF
Differential Output Resistance		10k	—	Ω
WDI Transition Frequency	WUS=Low	125	—	kHz
Read Mode (Vin is referenced to Vct)				
Differential Voltage Gain	Vin = 1mVpp @ 300kHz Z_L = 1kohm per side	80	120	V/V
Bandwidth (-3dB)	Z_S<5Ω, Vin = 1mVpp	30	—	MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0	—	2.1	nV/√Hz
Differential Input Capacitance	f = 5MHz	—	23	pF
Differential Input Resistance	f = 5MHz	2k	—	Ω
Input Bias Current (per side)		—	45	μA
Dynamic Range	DC input voltage where gain falls by 10% (tested with .5mVpp input @ 300 kHZ)	-2.0	2.0	mV
Common Mode Rejection Ratio	Vcm =Vct +100mV	50	—	dB
Power Supply Rejection Ratio	100mVpp on V5 or V12, f = 5MHz	45	—	dB
Channel Separation	Unselected channels driven with Vin = 100mVpp, f = 5MHz	45	—	dB
Output Offset Voltage		-480	+480	mV
Common Mode Output Voltage		5.0	7.0	V
Single Ended Output Resistance	f = 5MHz	—	30	Ω
Switching Characteristics T_J=25°C, I_w=35 mA, Lh=10vH, Rd=750Ω, f(Data)=5MHz				
Read to Write Transition Time	Delay to 90% of Write Current	—	1.0	μS
Write to Read Transition Time	Delay to 90% of 100mV 10MHz Read Signal Envelope Write Current Delay to 10%	—	1.0	μS
Head Select Switching Delay	Delay to 90% of 100mV 10MHz Read Signal Envelope	—	1.0	μS
Chip Disable Transition Time Read/Write to Idle Idle to Read/Write	Delay to 90% Decay of Write Current Delay to 90% of Write Current or to 90% of 100mV 10MHz read signal envelope	—	1.0	μS
Head Current Transition Time	IW = 35mA, Lh = 0, Rh = 0 10% to 90% points	—	20	nS
Unsafe to Safe Delay After Write Data Begins	IW = 20mA, Lh = 10μH	—	1.0	μS
Safe to Unsafe Delay	IW = 35mA, Lh = 10μH	1.6	8.0	μS
Head Current Switching Delay a) Time b) Asymmetry	35mA, Lh = 0μH, Rh = 0 50% VIL input to 50% output WDI has 50% Duty Cycle and 1nS Rise/Fall time	— —	25 2	nS nS

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-117-2DW	18 Lead SO Wide
CS-117-2N	18 Lead PDIP
CS-117-4DW	24 Lead SO Wide
CS-117-4N	24 Lead PDIP
CS-117-6DW	28 Lead SO Wide
CS-117-6FN	28 Lead PLCC
CS-117-6N	28 Lead PDIP

WITH INTERNAL DAMPING RESISTORS

CS-117-2RDW	18 Lead SO Wide
CS-117-2RN	18 Lead PDIP
CS-117-4RDW	24 Lead SO Wide
CS-117-4RN	24 Lead PDIP
CS-117-6RDW	28 Lead SO Wide
CS-117-6RFN	28 Lead PLCC
CS-117-6RN	28 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

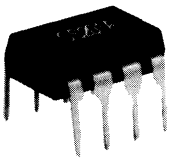
WINCHESTER SERVO PREAMP

CS-201A ™

DESCRIPTION

The CS-201A is a low noise servo preamplifier for use with ferrite heads. The CS-201A is an improved replacement for the CS-101A. Improvements include lower noise, wider bandwidth and lower current drain.

The CS-201A is pin compatible with the CS-101A and CS-116.



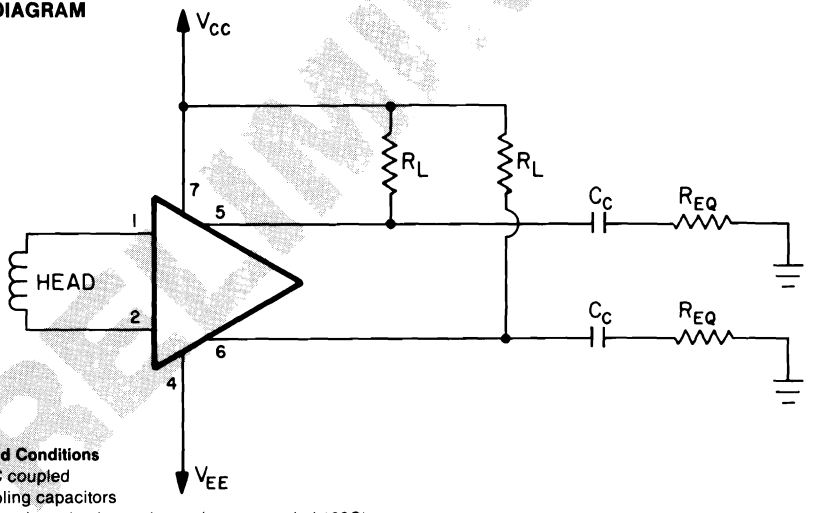
FEATURES:

- 50 MHz bandwidth
- Operates from any of three standard supply voltages:
  - 8.3V (IBM Compatible)
  - 10.0V
  - 12.0V
- Available in 8 pin plastic DIP, 8 pin CERDIP, or SO8

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{CC}-V_{EE})	14V
Differential Input Voltage	5V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	0°C to 70°C

CONNECTION DIAGRAM



Recommended Load Conditions

1. Input must be AC coupled
2. C_C's are AC coupling capacitors
3. R_L's are DC bias and termination resistors, (recommended 130Ω)
4. R_{EQ} represents equivalent load resistance
5. For gain calculations $R_P = \frac{R_L \cdot R_{EQ}}{R_L + R_{EQ}}$
6. Differential gain = 0.72 R_p (±18%) (R_p in Ω)
7. Ceramic capacitors (0.1 μ F) are recommended for good power supply noise filtering

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS T_A = 25°C, (V_{CC}-V_{EE}) = 7V to 13.2V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain (Differential)		80	100	120	V/V
Bandwidth (3dB)	Vin = 2mV	30	50	—	MHz
Input Resistance		1040	1300	1560	Ω
Input Capacitance		—	20	30	pF
Input Dynamic Range		3	—	—	mV
Power Supply current	(V_{CC}-V_{EE}) = 12V	—	20	25	mA
Output Offset (Differential)	R_s = 0, R_L = 130Ω	—	—	200	mV
Equivalent Input Noise	BW = 4MHz (Note 1)	—	0.7	1.0	nV/HZ
PSRR, Input Referred	R_s =0, f ≤5MHz	60	70	—	dB
Gain Sensitivity (Supply)	(V_{CC}-V_{EE}) = ±10%	—	±0.5	—	%/V
Gain Sensitivity (Temp.)	T_A = 25°C to 70°C, R_L = 130Ω	—	-0.1	—	%/C
CMRR, Input Referred	f ≤5MHz	60	70	—	dB

Recommended Operating Conditions	Min.	Typ.	Max.	Units
Supply Voltage (V_{CC}-V_{EE})	7.45 9.0 10.8	8.3 10.0 12.0	9.15 11.0 13.2	V V V
Input Signal Vi	—	2	—	mVpp
Ambient Temp. T_A	0	—	70	°C

Note 1: 1n/V/root Hz and a bandwidth of 4 MHz equals 2uVRMS.

3

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-201AN	8 Lead PDIP
CS-201AJ	8 Lead CDIP
CS-201AD	8 Lead SO

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-279

FLOPPY DISK LOGIC CIRCUIT and STEPPER MOTOR DRIVER

DESCRIPTION

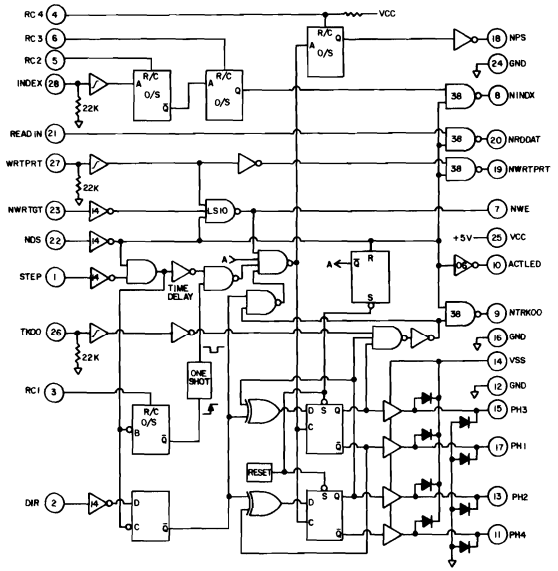
The CS279 is a floppy disk logic circuit with on chip bipolar Stepper Motor Drivers and clamp diodes. It provides all the logic functions needed for a standard disk drive. The CS279 is compatible with the CS570, CS3471/CS3470A or other Read/Write circuits. The CS279 incorporates Schmitt Trigger inputs for clean operation. The CS279 also has high current open collector outputs capable of connecting directly back to the host computer or interface.

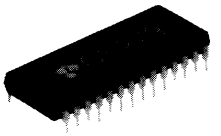
The three comparators on the circuit can be connected to photo sensors or switches to detect INDEX PULSES, TRACK-00 and WRITE PROTECTION. An on chip pull-down resistor provides a current path for the sensors so no additional components are necessary.

The Stepper Logic is capable of full or half stepping. An on chip, externally programmable one shot determines the time delay for the ghost pulse. This can easily be defeated by grounding the one shot pin. The direction input allows the circuit to step the motor in or out. Two high current bridge outputs are provided and can be directly connected to the bipolar stepper motor. On chip diodes provide the protection needed for the IC. This bipolar stepper motor driver is capable of driving up to 275mA per phase. A power saving circuit is provided and may be used to reduce the power consumption when the motor has finished stepping. Three grounds have been used on the chip to eliminate cross-talk between the stepper driver and the rest of the circuit.

The CS279 also has the necessary logic to inhibit the stepper circuit during the write mode. The write enable output only goes low when all the requirements of writing are met.

FUNCTIONAL BLOCK DIAGRAM

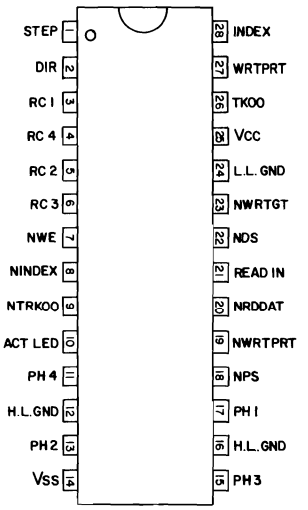




FEATURES:

- Stepper Logic, Full or Half Stepping
- On Chip Bipolar Stepper Motor Driver, Up to 275mA
- On Chip Clamp Diodes
- Power Saving Circuitry
- Direct Connection of Sensors Such as INDEX, TRACK-00 and WRITE PROTECT
- High Current Outputs for Direct Connection to the Host Controller
- LED Output Driver, Active During Drive Select
- Bipolar Linear/I^2L Technology

PIN CONNECTIONS (TOP VIEW)



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNITS
Supply Voltage	V_{CC} V_{SS}	7.0 15.0	Volts Volts
Input Voltage	V_{IN}	-.3 to Vcc +.3	Volts
Storage Temperature	Tstg	-40 to +150	C
Operating Temperature	Ta	0 to 70	C
Power Dissipation (Continuous, TA=50C)	Pd	2.0	Watts

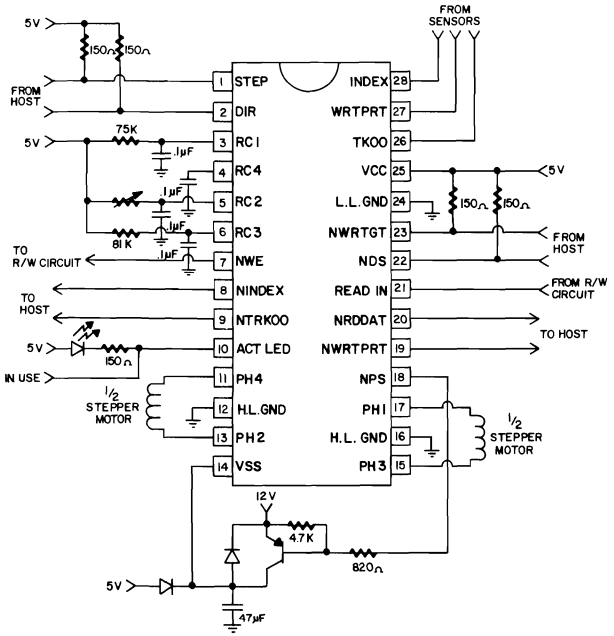
ELECTRICAL CHARACTERISTICS (Unless otherwise specified Vcc=5.0 Volts; Vss=12.0 Volts, Ta=25C)

PARAMETER	SYMBOL	PIN #'s	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics							
Logic Supply	V_{CC}	25		4.5		5.5	Volts
Stepper Supply	V_{SS}	14		4.00		13.2	Volts
Logic Current	I_{CC}	25				150	mA
Stepper Supply	I_{SS}	14	No load			75	mA
Rising Edge Schmitt Trip Point	VST+	1, 2, 22, 23		1.4		2.0	Volts
Falling Edge Schmitt Trip Point	VST-	1, 2, 22, 23		.5		1.0	Volts
Schmitt Hysterisis	VSHYS	1, 2, 22, 23		400		800	mVolts
High Level Schmitt Input Current	ISIH	1, 2, 22, 23	V_{IN}=2.7 V			20	μA
Low Level Schmitt Input Current	ISIL	1, 2, 22, 23	V_{IN}=0.4 V			-400	μA
Rising Comparator Trip Point	VCT+	26, 27, 28		1.6		2.2	Volts
Falling Comparator Trip Point	VCT-	26, 27, 28		1.1		1.7	Volts
Comparator Hysterisis (Note 5)	VCHYS			200		400	mVolts
Comparator Pulldown (Note 5)	RCIN			13		29.7	Kohms
Read in High Trip Point	VRIH	21		2			Volts
Read in Low Trip Point	VRIL	21				.8	Volts
Read in High Level Input Current	IRIH	21	V_{IN}=2.7V			20	μA
Read in Low Level Input Current	IRIL	21	V_{IN}=0.4V			-1.6	mA
Open Collector Output High Leakage Current	IOCHO	8, 9, 18, 19, 20	V_{OH}=5V			250	μA
Open Collector Output Voltage	VOCOL	8, 9, 18, 19, 20	I_O=40mA			.4	Volts
NWE Output High Voltage	VNWEOH	7	I_O=-400μA	2.7	3.4		Volts
NWE Output Low Voltage	VNWEOL	7	I_O=4mA			.4	Volts
Total Phase Output Saturation Voltage	VPH_{SAT}	11, 13, 15, 17	I_{OUT}=±275mA			3.4	Volts
Positive Phase Clamp	VO+	11, 13, 15, 17	I_{OUT}=275mA			2.0	Volts
Negative Phase Clamp	VO-	11, 13, 15, 17	I_{OUT}=-275mA	-2.0			Volts
AC Characteristics							
Power Save Pulse Width (Note 1)	PPS	4	C4=.1μF	30	50	125	msec
Index Pulse Width (Note 2)	PIP	6	R3=81K C3=.1μf	2.8		4.3	msec
Index to Data Pulse Width (Note 3)	PID	5	R2=1.25K to 50K C2=.1μf	50		2000	μsec
Step One Shot Pulse Width (Note 4)	PS	3	R1=75K C1=.1μf	2.4	3	3.6	msec
Read in Pulse	PRI	20, 21		1			μsec
NRDDAT Propagation Delay	TD	20, 21	V_{OUT}, Low to High V_{OUT}, High to Low			750 100	nsec nsec
Input Step Pulse Width	PSI	1		1			μsec
V_{SS} & V_{CC} Supply Ripply	VR	14, 25	1Hz<f<1MHz			100	mVolt

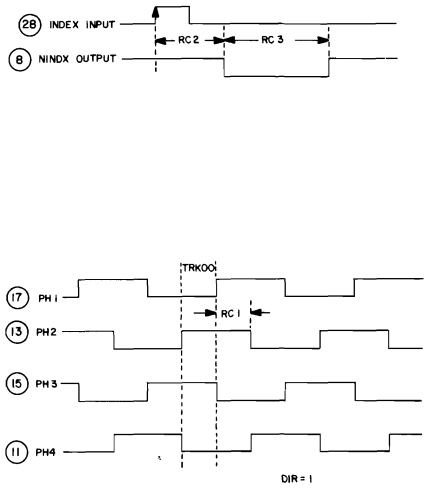
1. Minimum Pulse Width is specified over the operating temperature range.
2. Index Pulse Width is specified over the operating temperature range.
3. Index to Data Pulse Width shall remain within ±50 μsec of room temperature value over the temperature range of 10C to 46C. Also the following equation is true: .320 RC ≤PW ≤.480 RC.
4. Step One Shot Pulse Width shall not vary by more than ±20% over the temperature range of 10C to 46C. Grounding the RC1 pin shall inhibit this function.
5. The input current at the positive threshold shall not vary more than 2000 PPM/°C over the normal operating range.

PIN DESCRIPTIONS

SYMBOL	PIN #	DESCRIPTION
Input Pins		
TKOO	26	**TRACK 00** is a comparator input with hysterisis. An internal 22K pull down resistor is provided. A "0" on this input causes NTRKOO output to go low.
WRTPRT	27	**WRITE PROTECT** is a comparator input with hysterisis. An internal 22K pulldown resistor is provided. A "0" on this input causes NWE to go high and NWRPRT to go low.
NWRTGT	23	**NOT WRITE GATE** is a Schmitt trigger input. A "0" on this input disables the stepper circuitry and causes a "0" on the NWE output.
NDS	22	**NOT DRIVE SELECT** is a Schmitt trigger input. A "0" on this input enables the IC.
INDEX	28	**INDEX** is a comparator input with a 22K pulldown resistor provided. A positive transition on this input fires the RC2 oneshot. After RC2 times out the RC3 oneshot fires during which time the NINDEX goes low.
DIR	2	**DIRECTION** is a Schmitt trigger input. The polarity of this input determines the direction which the stepper motor moves. This signal is latched in by the step signal.
STEP	1	**STEP** input is a Schmitt input. The positive going trailing edge clocks the direction flip-flop, steps the stepper motor and triggers the stepper one shot.
READIN	21	**READ INPUT** input is a TTL input. A "1" on this input causes a low condition on the NRDDAT output.
RC1	3	**RC1** is the stepper one shot. This one shot shall trigger on the trailing edge of the step pulse. If RC1 is grounded the one shot is inhibited.
RC2	2	**RC2** is the Index to Data one shot. This one shot shall trigger on the leading edge of the Index pulse.
RC3	6	**RC3** is the Index pulse width one shot. This one shot shall trigger on the trailing edge of the Index to Data one shot.
RC4	4	**RC4** is the Power Save one shot. This one shot shall trigger on the trailing edge of the Step pulse.
VCC	25	**VCC** is the +5 volt supply voltage to the IC.
VSS	14	**VSS** is the +12 volt supply voltage to the stepper motor outputs.
HGND	12, 16	**HIGH GROUND** Hi current output ground.
LGND	24	**LOW GROUND** Low current logic ground.
Output Pins		
NWE	7	**NOT WRITE ENABLE** is a TTL type output. This output turns on when NWRTGT is a "0" and WRTPRT is a "1"
NTRKOO	9	**NOT TRACK 00** is a 40 mA open collector output. This output is turned on when TKOO is a "0"
NPS	18	**NOT POWER SAVE** is a 40 mA open collector output. This output is turned on when the Power Save one shot triggers during the step Pulse.
NINDEX	8	**NOT INDEX** is a 40 mA open collector output. This output turns on when the Index Pulse Width one shot triggers.
ACTLED	10	**THE ACTIVITY LED** is a 30 mA open collector output. This output turns on when the NDS input is low.
NWRPRT	19	**NOT WRITE PROTECT** is a 40 mA open collector output. This output turns on when WRTPRT is low.
NRDDAT	20	**NOT READ DATA** is a 40 mA open collector output. This output turns on when READIN is high.
PH1	17	**PHASE 1** is a 275 mA push pull output. This output reflects the $\overline{Q}$ of one of the stepper motor flip-flops.
PH2	13	**PHASE 2** is a 275 mA push pull output. This output reflects the Q of one of the stepper motor flip-flops.
PH3	15	**PHASE 3** is a 275 mA push pull output. This output reflects the Q of one of the stepper motor flip-flops.
PH4	11	**PHASE 4** is a 275 mA push pull output. This output reflects the $\overline{Q}$ of one of the stepper motor flip-flops.



TYPICAL APPLICATION



TIMING DIAGRAM

3

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-279	28 Lead PDIP

CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

2, 4, 6 CHANNEL

READ/WRITE CIRCUIT

CS-510A/ 510AR ™

DESCRIPTION

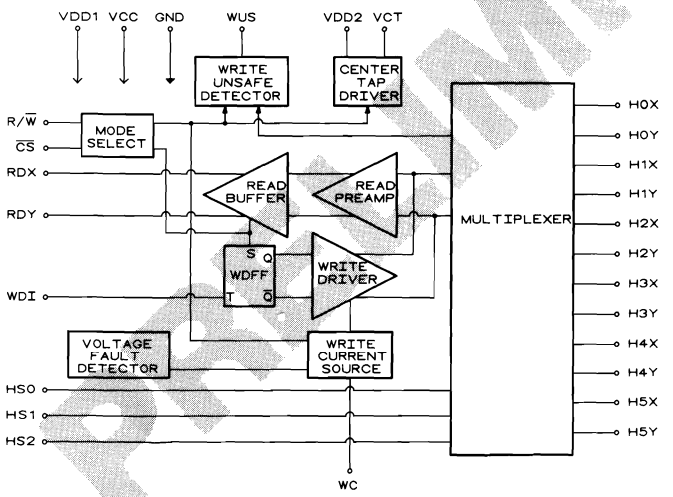
The CS-510A is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection circuitry for as many as 6 channels. The CS-510A requires +5V and +12V power supplies and is available in a variety of packages.

The CS-510AR performs the same function as the CS-510A with the addition of internal 750 Ω damping resistors.

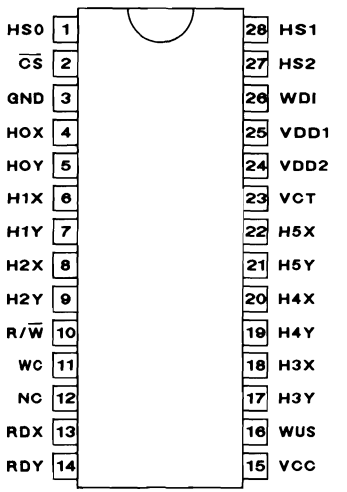
FEATURES:

- +5V, +12V power supplies
- Single or multi-platter Winchester drives
- Designed for center-tapped ferrite heads
- Programmable write current source
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals
- Power supply fault protection
- 1.5 nV/$\sqrt{Hz}$ maximum input noise voltage

BLOCK DIAGRAM



PIN CONNECTIONS
(6-Channel)



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

CIRCUIT OPERATION

The CS-510A has the ability to address up to 6 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control are accomplished using the HSn, $\overline{CS}$, & R/$\overline{W}$ inputs as in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0=Low level 1=High level X=Don't care

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the CS-510A as a current switch and activates the Write Unsafe Detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc connected from pin WC to GND and is given by:

Iw=K/Rwc, where K=Write Current Constant

Write Unsafe Detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe, WUS, open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in Read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further ensure Data security, a Voltage Fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance Write to Read recovery time the change in RDX, RDY comon mode voltage is minimized by biasing these outputs to a level within the read mode range when in Write Mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 and VDD2. Optimum resistor value is 150Ω x 40/Iw (Iw in mA). At low write currents, (<15mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the CS-510A as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head paths. These ouputs should be AC coupled to the load. The internal write current source is gated off in Read mode eliminating the need for any external gating.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the Write Current programming resistor to be common to all devices.

TABLE 3: PIN DESCRIPTIONS

SYMBOL	I/O	NAME-DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	ChipSelect: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read Mode
WUS	O	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X/H0Y-H5Y	I/O	X, Y head connections
RDX, RDY	O	X, Y Read Data: Differential read signal out
WC	I	Write Current: used to set the magnitude of the write current
VCT	I	Voltage Center Tap: voltage source for head center tap

PIN DESCRIPTIONS (Continued)

SYMBOL	I/O	NAME-DESCRIPTION
VCC	I	+5V
VDD1	I	+12V
VDD2	I	Positive power supply for the Center Tap Voltage source
GND	I	Ground

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND). Currents into device are positive.

PARAMETER		VALUE	UNITS
DC Supply Voltage	(VDD1)	-0.3 to +14	VDC
	(VDD2)	-0.3 to +14	VDC
	(VCC)	-0.3 to +6	VDC
Digital Input Voltage Range (VIN)		-0.3 to VCC +0.3	VDC
Head Port Voltage Range (VH)		-0.3 to VDD1 +0.3	VDC
WUS Pin Voltage Range (Vwus)		-0.3 to +14	VDC
Write Current (IW) Zero Peak		60	mA
Output Current	RDX, RDY (Io)	-10	mA
	VCT	-60	mA
	WUS	+12	mA
Storage Temperature Range (Tstg)		-65 to 150	°C
Lead Temperature PDIP (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 Sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Supply Voltage	(VDD1)		10.8	12.0	13.2	VDC
	(VCC)		4.5	5.0	5.5	VDC
Head Inductance (Lh)			5		15	μH
Damping Resistor (RD) (510A Only)			500		2000	ohms
RCT Resistor (RCT)*(¼ Watt)		Iw=40mA	142	150	158	ohms
Write Current (IW)			10		40	mA
Junction Temperature Range (Tj)			+25		+125	°C

* For Iw=40mA, At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤Tj≤+125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
VCC Supply Current	Read/Idle	Read/Idle Mode			35	mA
	Write	Write Mode			30	mA
VDD Supply Current	Idle	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read	Read Mode			35	mA
	Write	Write Mode			20+Iw	mA
Power Dissipation	Idle	Tj=+125°C Idle Mode			400	mW
	Read	Read Mode			600	mW
	Write	Write Mode, IW=40mA, RCT=0Ω			870	mW

DC CHARACTERISTICS (Continued)

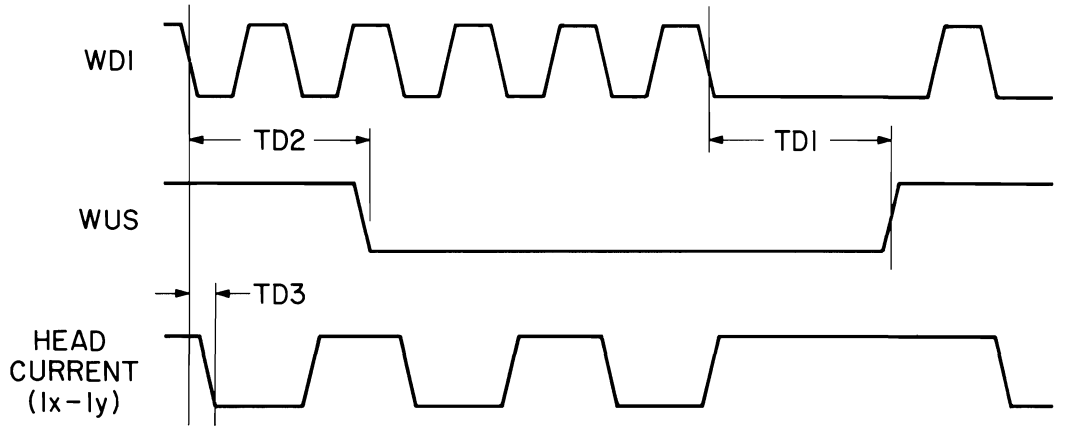
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O					
VIL, Input Low Voltage				0.8	VDC
VIH, Input High Voltage		2.0			VDC
IIL, Input Low Current	VIL=0.8V	-0.4			mA
IIH, Input High Current	VIH=2.0V			100	μA
VOL, WUS Output, Low Voltage	IOL=8mA			0.5	VDC
IOH, WUS Output High current	VOH=5.0V			100	μA
WRITE MODE					
Center Tap Voltage (VCT)	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, 0≤VCC≤3.7V 0≤VDD1≤8.7V	-200		200	μA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	μA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY=6V Write/Idle Mode	-100		100	μA
READ MODE					
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0≤VCC≤5.5V 0≤VDD1≤13.2V	-200		200	μA
Input Bias Current (per side)				45	μA
Output Offset Voltage	Read Mode	-440		+440	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤Tj≤125°C, IW=35mA, Lh=10μH, Rd=750Ω, f(WDI)=5MHz, CL (RDX, RDY)≤20pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE					
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	510A	10K			Ω
	510AR	600		960	Ω
WDI Transition Frequency	WUS=low	250			KHz
READ MODE					
Differential Voltage Gain	Vin=1mVpp@300kHz RL(RDX), RL(RDY)=1KΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin=Vi+0.5mVpp@300kHz	-3		+3	mV

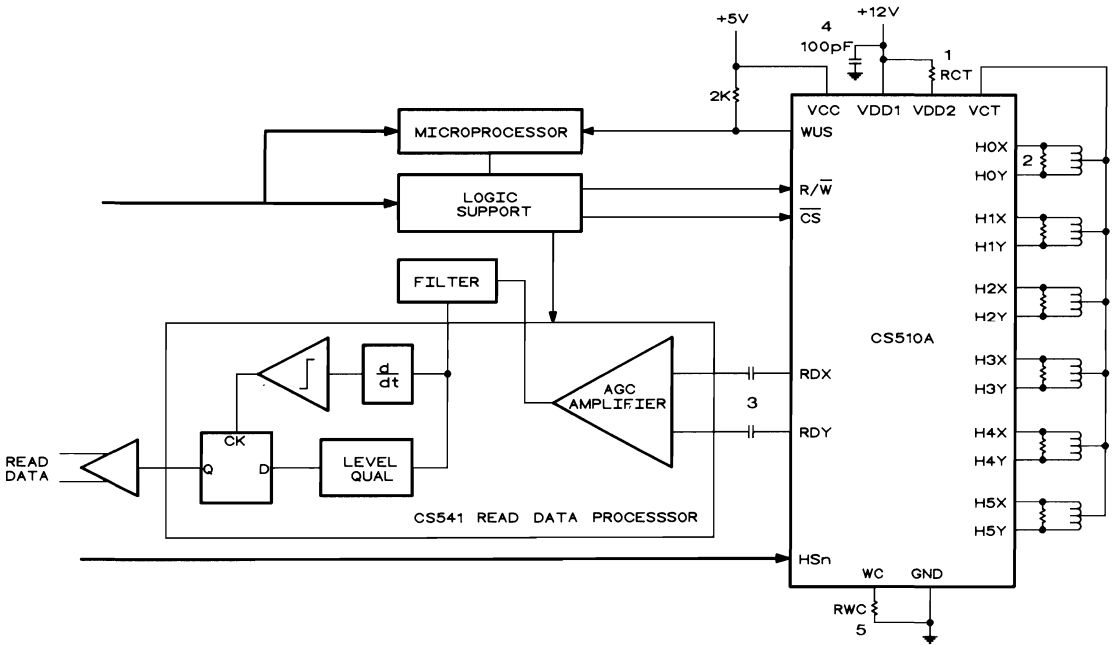
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
READ MODE (Cont'd.)					
Bandwidth (-3db)	Zs<5Ω, Vin=1mVpp	30			MHz
Input Noise Voltage	BW=15MHz, Lh=0 Rh=0			1.5	nV/$\sqrt{Hz}$
Differential Input Capacitance	f=5MHz			20	pF
Differential Input Resistance	f=5MHz 510A	2K			Ω
	510AR	460		860	Ω
Common Mode Rejection Ratio	Vcm=VCT+100mVpp @5MHz	50			db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC	45			db
Channel Separation	Unselected Channels: Vin=100mVpp@ 5MHz & Selected Channel: Vin=0mVpp	45			db
Single Ended Output Resistance	f=5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	2.1			mA
SWITCHING CHARACTERISTICS					
R/$\overline{W}$: R/$\overline{W}$ to Write	Delay to 90% of Write Current			1.0	μS
R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current			1.0	μS
$\overline{CS}$: $\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope			1.0	μS
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	μS
HS0 HS1 to any Head HS2	Delay to 90% of 100mV 10MHz Read Signal Envelope			1.0	μS
WUS: Safe to Unsafe-TD1	Iw=35mA	1.6		8.0	μS
Unsafe to Safe-TD2				1.0	μS
Head Current: Prop. Delay-TD3	Lh=0μH, Rh=0Ω From 50% Points			25	nS
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	nS
Rise/Fall Time	10%-90% Points			20	nS



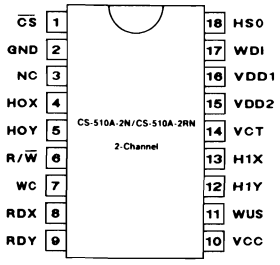
WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

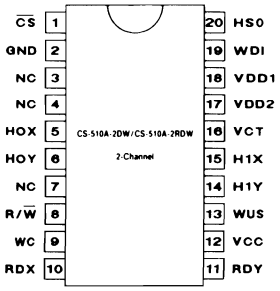


NOTES:
1. An external resistor, RCT, given by; RCT=150 (40/Iw) where Iw is the zero peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 510AR versions.
3. Limit DC current from RDX and RDY to 100 μA and load capacitance to 20pF. In multi-chip application these outputs can be wire-or'd.
4. The power bypassing capacitor must be located close to the 510A with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 510A. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

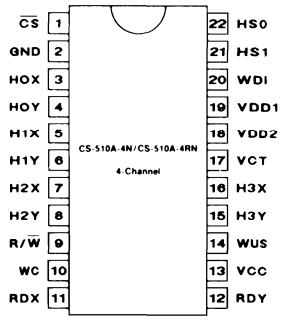
PIN CONNECTIONS



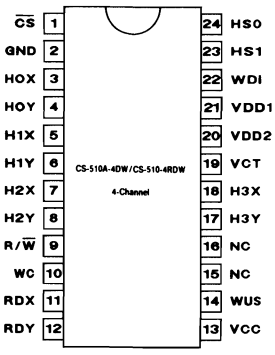
18-LEAD PDIP



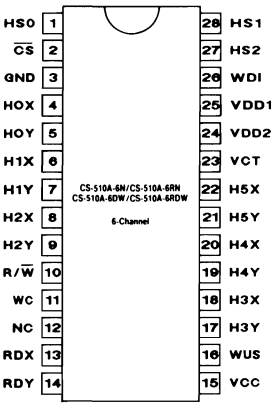
20-LEAD SO



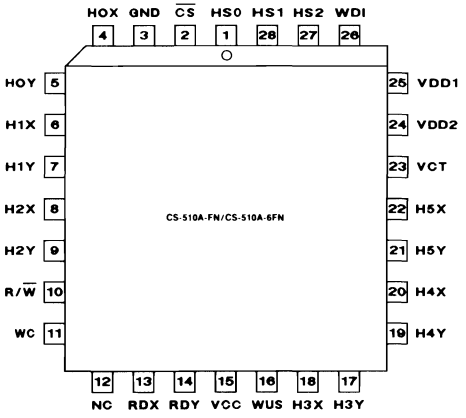
22-LEAD PDIP



24-LEAD SO



28-LEAD PDIP/SO



28-LEAD PLCC

THERMAL CHARACTERISTICS

PACKAGE	Øja
18-LEAD PDIP	140°C/W
20-LEAD SO	95°C/W
22-LEAD PDIP	60°C/W
24-LEAD SO	85°C/W

PACKAGE	Øja
28-LEAD PLCC	65°C/W
PDIP	100°C/W
SO	80°C/W

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-510A-2N	18 lead PDIP
CS-510A-2DW	20 lead SO
CS-510A-4N	22 lead DDIP
CS-510A-4DW	24 lead SO
CS-510A-6N	28 lead PDIP
CS-510A-6FN	28 lead PLCC
CS-510A-6DW	28 lead SO
with internal damping resistors	
CS-510A-2RN	18 lead PDIP
CS-510A-2RDW	20 lead SO
CS-510A-4RN	22 lead DDIP
CS-510A-4RDW	24 lead SO
CS-510A-6RN	28 lead PDIP
CS-510A-6RFN	28 lead PLCC
CS-510A-6RDW	28 lead SO

3

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

4, 6, 8-CHANNEL FERRITE HIGH PERFORMANCE

READ/WRITE CIRCUIT

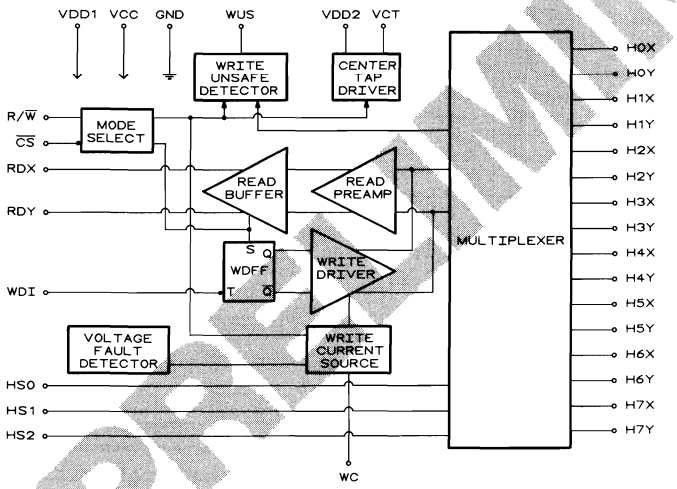
DESCRIPTION

The CS-511 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection circuitry for as many as 8 channels. The CS-511 requires +5V and +12V power supplies and is available in a variety of packages. The CS-511R performs the same function as the CS-511 with the addition of internal 750Ω damping resistors.

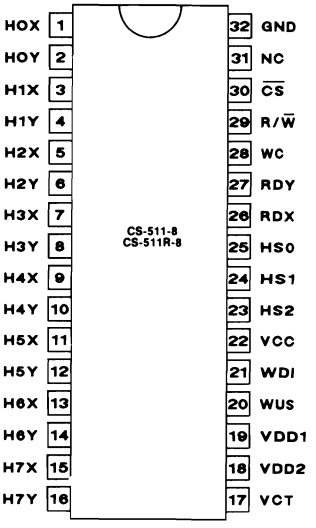
FEATURES:

- High Peformance:
  - Read mode gain = 100 V/V
  - Input noise = 1.5 nV/$\sqrt{Hz}$ maximum
  - Input capacitance = 20 pF
  - Write current range = 10 mA to 40 mA
- Enhanced system write to read recovery time
- Power supply fault protection
- Designed for center-tapped ferrite heads
- Programmable write current source
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control supplies
- +5V, +12V power supplies

BLOCK DIAGRAM



PIN CONNECTIONS
32 Lead SODW



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

CIRCUIT OPERATION

The CS-511 gives the user the ability to address up to 8 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

O = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the CS-511 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output :

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 120Ω x 40/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the CS-511 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X, H0Y-H7Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center-tap voltage source
GND	-	Ground

* When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC +0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 +0.3	VDC
WUS Pin Voltage Range	V_{WUS}	-0.3 to +14	VDC
Write Current Zero Peak	IW	60	mA
RDX, RDy Output Current	I_O	-10	mA
VCT Output Current	I_{VCT}	-60	mA
WUS Output Current	I_{WUS}	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, Flat Pack (10 sec Soldering)		260	°C
Package Temperature PLCC (20 sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	μH
Damping Resistor	RD	CS-511 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 40 mA	114	120	126	Ω
Write Current	IW		10		40	mA
Junction Temperature Range	Tj		+25		+135	°C

* For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = + 125°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, IW = 40 mA, RCT = 0Ω			800	mW
	Write Mode, IW = 40 mA RCT = 120Ω			610	mW

DC CHARACTERISTICS (Continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	μA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	μA

3

WRITE MODE

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Center Tap Voltage	VCT	Write Mode		6.0		VDC
Head Current (per side)		Write Mode, $0 \leq VCC \leq 3.7V$, $0 \leq VDD1 \leq 8.7V$	-200		200	μA
Write Current Range			10		40	mA
Write Current Constant "K"			2.375		2.625	
Iwc to Head Current Gain				0.99		mA/mA
Unselected Head Leakage Current					85	μA
RDX, RDY Output Offset Voltage		Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage		Write/Idle Mode		5.3		VDC
RDX, RDY Leakage		RDX, RDY = 6V Write/Idle Mode	-100		100	μA

READ MODE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode $0 \leq VCC \leq 5.5V$ $0 \leq VDD1 \leq 13.2V$	-200		200	μA
Input Bias Current (per side)				45	μA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 10μH, Rd = 750Ω CS-511 only, f(WDI) = 5 MHz, CL (RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	CS-511	10K			Ω
	CS-511R	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential voltage Gain	Vin = 1mVpp @ 300kHz, RL(RDX), RL(RDY) = 1 KΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 kHz	-3		+3	mV
Bandwidth (-3dB)	$\|Zs\| < 5\Omega$, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	CS-511, f = 5 MHz	2K			Ω
Differential Input Resistance	CS-511R, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin = 100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			1.0	μs
R/$\overline{W}$ To Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	μs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	μs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	μs
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	μs
WUS, Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	μs
WUS, Unsafe to Safe - TD2	Iw = 35 mA			1.0	μs
Head Current (Lh = 0 μH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time			2	ns
Rise/Fall Time	10%-90% Points			20	ns

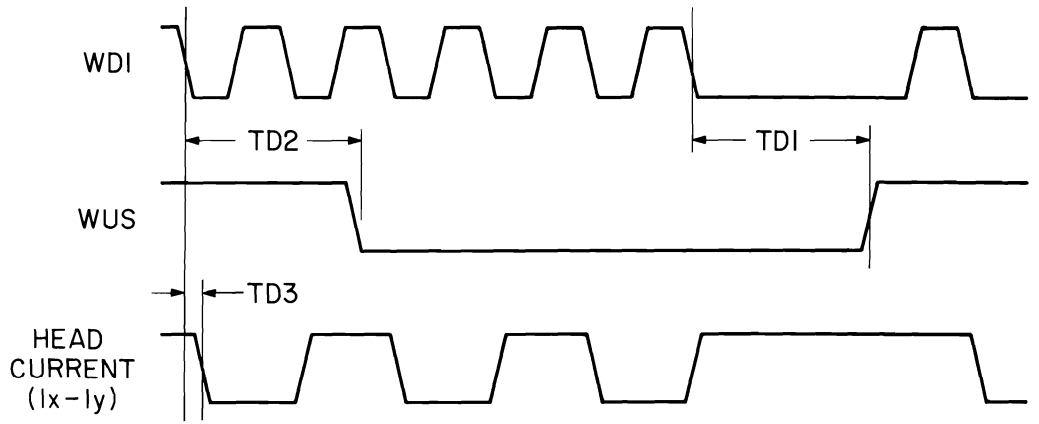
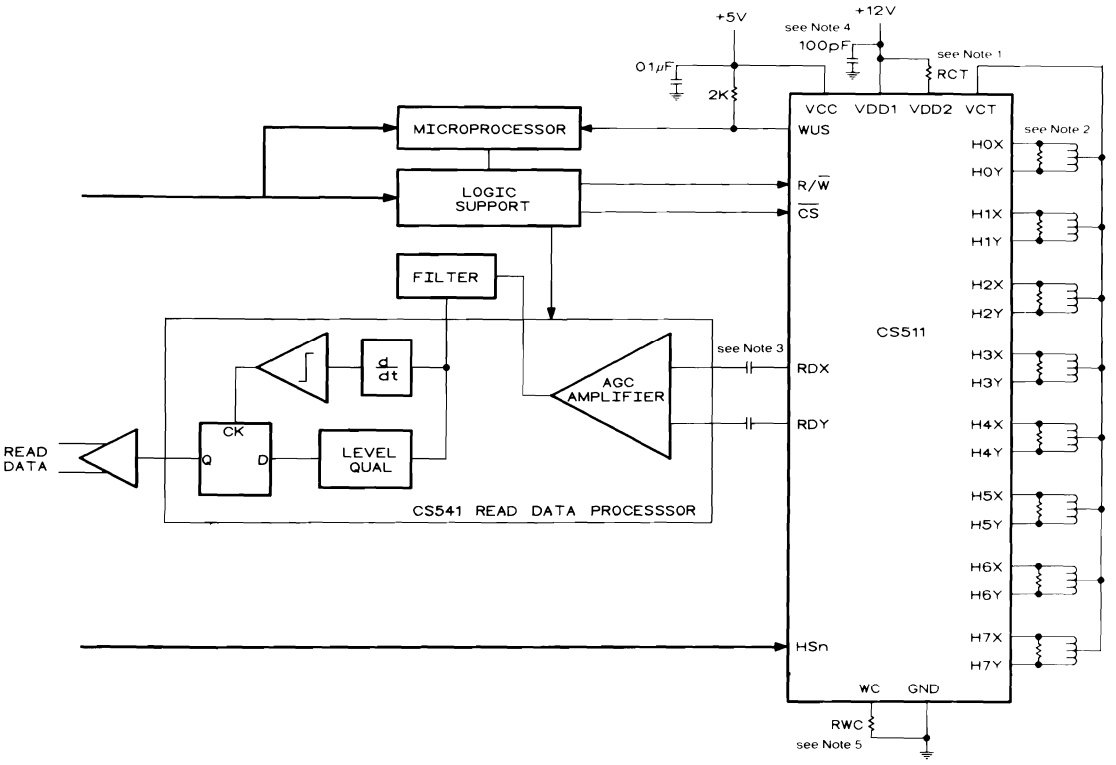


FIGURE 1: WRITE MODE TIMING DIAGRAM

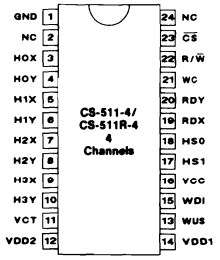
APPLICATIONS INFORMATION



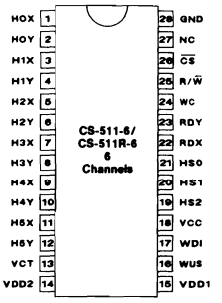
NOTES

1. An external resistor, RCT, given by; RCT = 120 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1
2. Damping resistors not required on CS-511R versions.
3. Limit DC current from RDX and RDY to 100 μA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the CS-511 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the CS-511. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

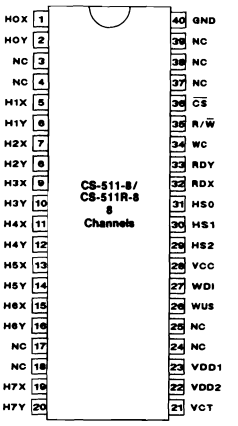
PACKAGE PIN DESIGNATIONS (Top View)



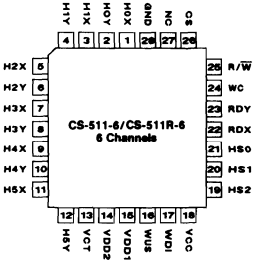
24-Lead



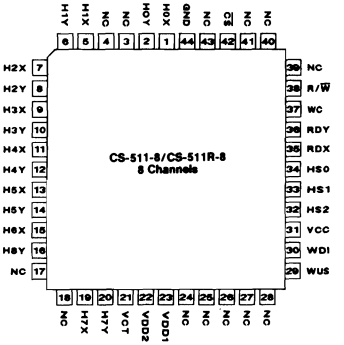
28-Lead SO



40-Lead PDIP



28-Lead PLCC



44-Lead PLCC

THERMAL CHARACTERISTICS

PACKAGE		Øja
24-LEAD	SO	75°C/W
28-LEAD	PLCC	63°C/W
28-LEAD	SO	70°C/W
32-LEAD	SO	65°C/W
40-LEAD	PDIP	42°C/W
44-LEAD	PLCC	46°C/W

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-511-4DW	24 lead SO
CS-511-6DW	28 lead SO
CS-511-6FN	28 lead PLCC
CS-511-8DW	32 lead SO
CS-511-8N	40 lead PDIP
CS-511-8FN	40 lead PLCC
with internal damping resistors	
CS-511-4RDW	24 lead SO
CS-511-6RDW	28 lead SO
CS-511-6RFN	28 lead PLCC
CS-511-8RDW	32 lead SO
CS-511-8RN	40 lead PDIP
CS-511-8RFN	40 lead PLCC

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

2, 4, 6-CHANNEL HIGH PERFORMANCE

READ/WRITE CIRCUIT

CS-514/
514R ™

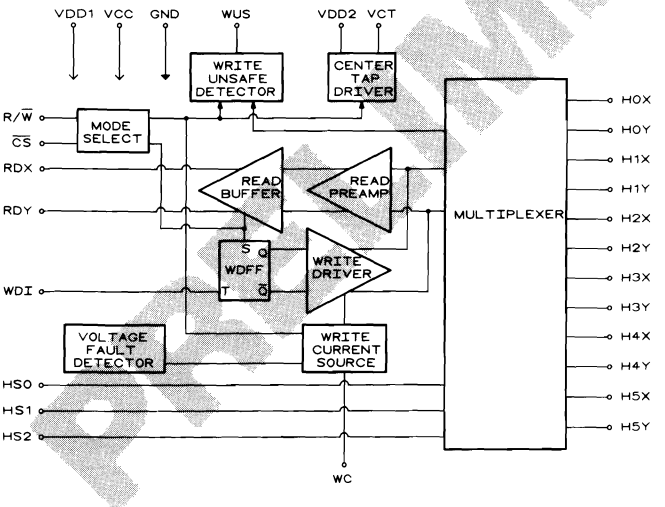
DESCRIPTION

The CS-514/514R Read/Write devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. The CS-514R option provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The CS-514 is available in a variety of package and channel configurations.

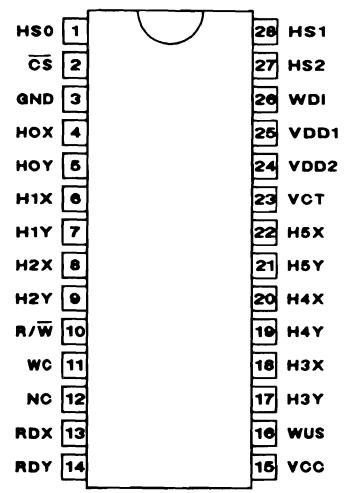
FEATURES:

- High Peformance:
  - -Read mode gain = 150 V/V
  - -Input noise = 1.5 nV/$\sqrt{Hz}$ max.
  - -Input capacitance = 20 pF max.
  - -Write current range = 10 mA to 40 mA
- Enhanced system write to read recovery time
- Power supply fault protection
- Plug compatible to the CS-117 & CS-510A
- Designed for center-tapped ferrite heads
- Programmable write current source
- Write unsafe detection
- TTL compatible control signals
- +5V, +12V power supplies

BLOCK DIAGRAM



PIN CONNECTIONS
28 LEAD SO



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

CIRCUIT OPERATION

The CS-514 addresses up to six center-tapped ferrite heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$, and R/$\overline{W}$, as shown in tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$, will force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0=Low level 1=High level X=Don't care

WRITE MODE

The write mode configures the CS-514 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant. In multiple device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in Read mode
- No write current

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the CS-514 as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	ChipSelect: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read Mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X/H0Y-H5Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y Read Data: Differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	—	Voltage Center Tap: voltage source for head center tap
VCC	—	+5V
VDD1	—	+12V
VDD2	—	Positive power supply for the center-tap voltage source
GND	—	Ground

* When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	(VDD1)	-0.3 to +14	VDC
	(VDD2)	-0.3 to +14	VDC
	(VCC)	-0.3 to +6	VDC
Digital Input Voltage Range (VIN)		-0.3 to VCC +0.3	VDC
Head Port Voltage Range (VH)		-0.3 to VDD1 +0.3	VDC
WUS Pin Voltage Range (Vwus)		-0.3 to +14	VDC
Write Current (O-pk)	Iw	60	mA
Output Current	RDX, RDY (Io)	-10	mA
	VCT	-60	mA
	WUS	+12	mA
Storage Temperature Range (Tstg)		-65 to 150	°C
Lead Temperature PDIP (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 Sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Supply Voltage	(VDD1)		10.8	12.0	13.2	VDC
	(VCC)		4.5	5.0	5.5	VDC
Head Inductance (Lh)			5		15	μH
Damping Resistor (RD) (514 Only)			500		2000	ohms
RCT Resistor (RCT)*(¼ Watt)		Iw=40mA	123	130	138	ohms
Write Current (IW)			10		40	mA
Junction Temperature Range (Tj)			+25		+125	°C

* For Iw=40mA, At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤Tj≤+135°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
VCC Supply Current	Read/Idle	Read/Idle Mode			35	mA
	Write	Write Mode			30	mA
VDD Supply Current	Idle	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read	Read Mode			35	mA
	Write	Write Mode			20+Iw	mA
Power Dissipation	Idle	Tj=+125°C Idle Mode			400	mW
	Read	Read Mode			600	mW
	Write	Write Mode, IW=40mA, RCT=0Ω			800	mW
	Write	Write Mode, IW=40mA, RCT=130Ω			600	mW

DC CHARACTERISTICS (Continued)

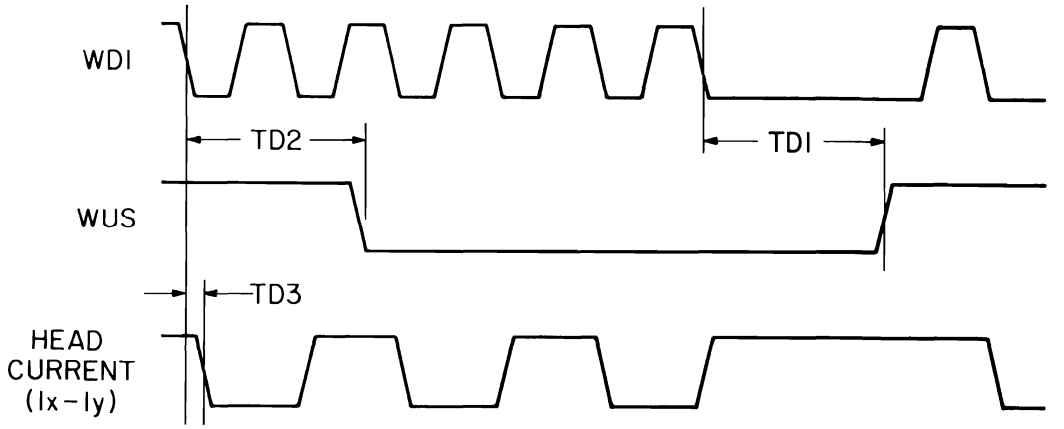
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O					
VIL, Input Low Voltage				0.8	VDC
VIH, Input High Voltage		2.0			VDC
IIL, Input Low Current	VIL=0.8V	-0.4			mA
IIH, Input High Current	VIH=2.0V			100	μA
VOL, WUS Output, Low Voltage	IOL=8mA			0.5	VDC
IOH, WUS Output High current	VOH=5.0V			100	μA
WRITE MODE					
Center Tap Voltage (VCT)	Write Mode		6.7		VDC
Head Current (per side)	Write Mode, 0≤VCC≤3.7V 0≤VDD1≤8.7V	-200		200	μA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	μA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY=6V Write/Idle Mode	-100		100	μA
READ MODE					
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0≤VCC≤5.5V 0≤VDD1≤13.2V	-200		200	μA
Input Bias Current (per side)				45	μA
Output Offset Voltage	Read Mode	-615		+615	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤Tj≤125°C, IW=35mA, Lh=10μH, Rd=750Ω, f(WDI)=5MHz, CL (RDX, RDY)≤20pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE					
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	514	10K			Ω
	514R	600		960	Ω
WDI Transition Frequency	WUS=low	250			KHz
READ MODE					
Differential Voltage Gain	Vin=1mVpp@300kHz ZL(RDX), ZL(RDY)=1KΩ	125		175	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin=Vi+0.5mVpp@300kHz	-2		+2	mV

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
READ MODE (Cont'd.)					
Bandwidth (-3db)	Zs<5Ω, Vin=1mVpp	30			MHz
Input Noise Voltage	BW=15MHz, Lh=0 Rh=0			1.5	nV/$\sqrt{Hz}$
Differential Input Capacitance	f=5MHz			20	pF
Differential Input Resistance	f=5MHz 514	3.2K			Ω
	514R	500		1000	Ω
Common Mode Rejection Ratio	Vcm=VCT+100mVpp @5MHz	50			db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC	45			db
Channel Separation	Unselected Channels: Vin=100mVpp@ 5MHz & Selected Channel: Vin=0mVpp	45			db
Single Ended Output Resistance	f=5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA
SWITCHING CHARACTERISTICS					
R/$\overline{W}$ to Write	Delay to 90% of Write Current			1.0	μS
R/$\overline{W}$ to Read	Delay to 90% of 100mV, 10MHz Read Signal Envelope or to 90% decay of Write Current			1.0	μS
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope			1.0	μS
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	μS
HS0-HS2 to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope			1.0	μS
WUS: Safe to Unsafe-TD1	Iw=35mA	1.6		8.0	μS
Unsafe to Safe-TD2				1.0	μS
Head Current Lh=0μH, Rh=0Ω					
Prop. Delay-TD3	From 50% Points			25	nS
Assymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	nS
Rise/Fall Time	10%-90% Points			20	nS



WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representaive of actual performance.

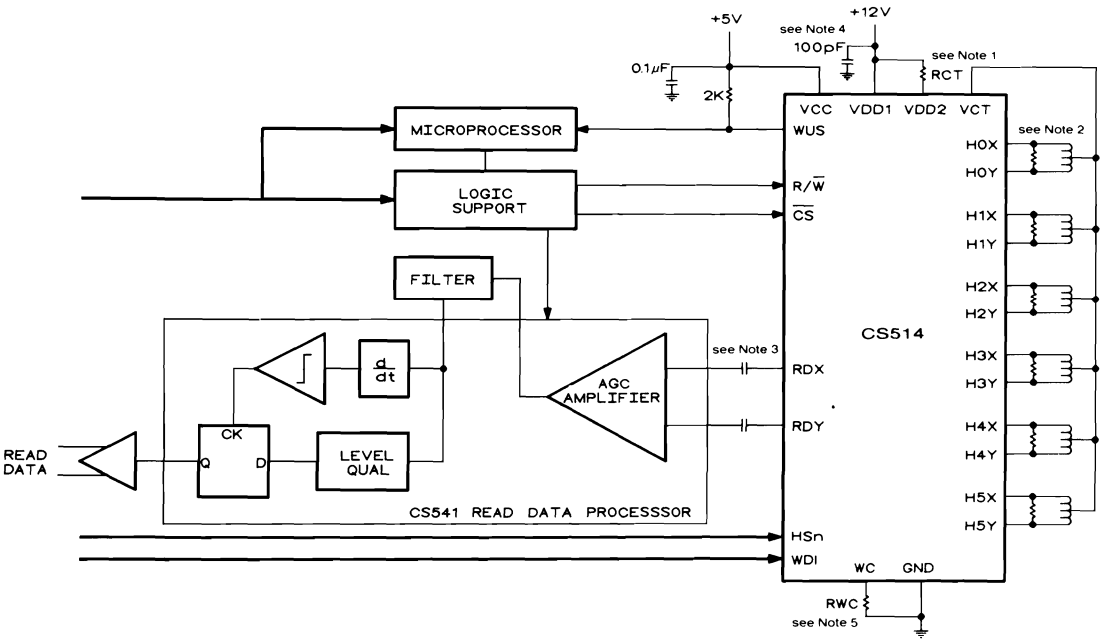
TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	514R	850	1000	Ω
	514	15.4	29.4	KΩ
Differential Input Capacitance (max.)		11.6	10.8	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	514R	500	620	Ω
	514	3.2	6.1	KΩ
Differential Input Capacitance (max.)		10.1	10.3	pF

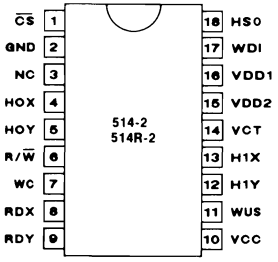
APPLICATIONS INFORMATION (continued)



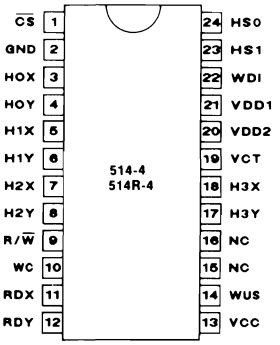
NOTES:

1. An external resistor, RCT, given by; RCT≤130 (40/Iw) where Iw is the zero peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1
2. Damping resistors not required on CS-514R versions.
3. Limit DC current from RDX and RDY to 100 μA and load capacitance to 20pF. In multi-chip application these outputs can be wire-or'd.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

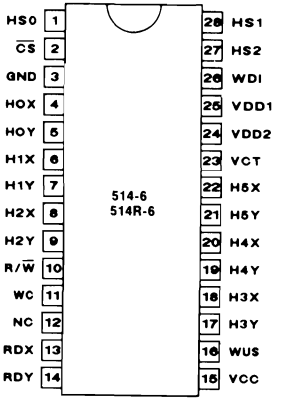
PIN CONNECTIONS



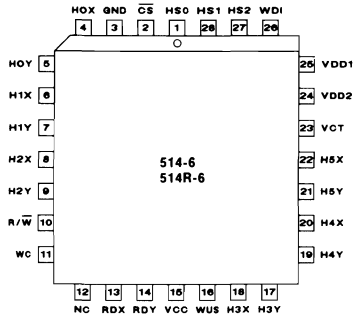
18-LEAD SO



24-LEAD SO



28-LEAD SO



28-LEAD PLCC

THERMAL CHARACTERISTICS

PACKAGE		Øja
18-LEAD	SO	100°C/W
24-LEAD	SO	85°C/W
28-LEAD	SO	80°C/W
28-LEAD	PLCC	65°C/W

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-514-2DW	18 lead SO
CS-514-4DW	24 lead SO
CS-514-6DW	28 lead SO
CS-514-6FN	28 lead PLCC
with internal damping resistors	
CS-514-2RDW	18 lead SO
CS-514-4RDW	24 lead SO
CS-514-6RDW	28 lead SO
CS-514-6RFN	28 lead PLCC

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

READ DATA PROCESSOR

CS-541™

DESCRIPTION

The CS-541 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals. The circuit will handle data rates up to 15 Megabits/sec.

In read mode the CS-541 provides amplification and qualification of head preamplifier outputs. Pulse qualification is achieved using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, Presenting a constant input level to the pulse qualification circuitry.

The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

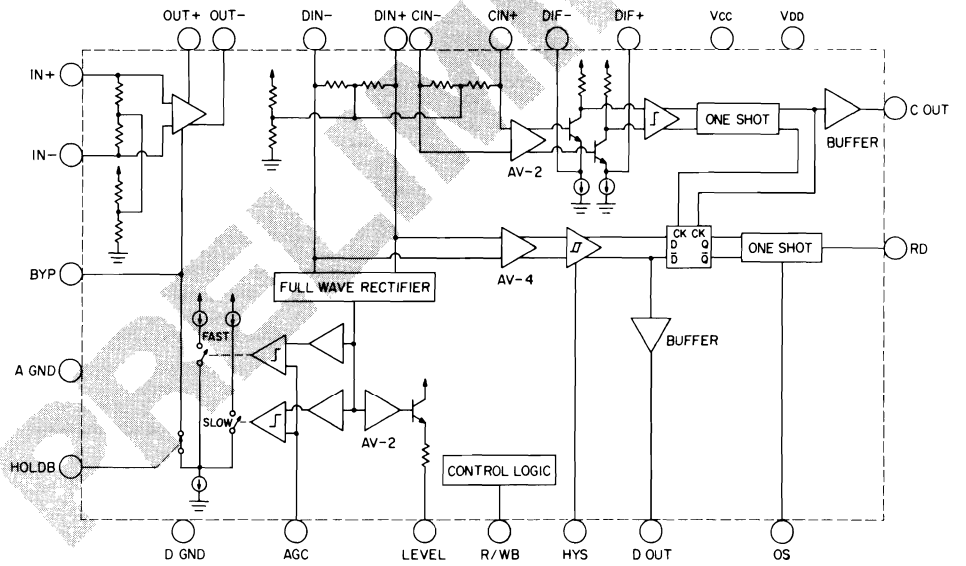
In write mode the circuitry is disabled and the AGC gain stage input impedance switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition.

The CS-541 requires +5V and +12V power supplies and is available in a 24 pin DIP and a 28 pin PLCC.

FEATURES:

- Level qualification supports high resolution MFM and RLL encoded data retrieval
- Wide bandwidth AGC input amplifier
- Supports data rates up to 15 megabits/sec
- Standard 12V ±10% and 5V ±10% supplies
- Supports embedded servo pattern decoding
- Write to read transient suppression
- Fast and slow AGC attack regions for fast transient recovery

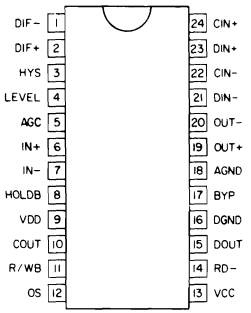
BLOCK DIAGRAM



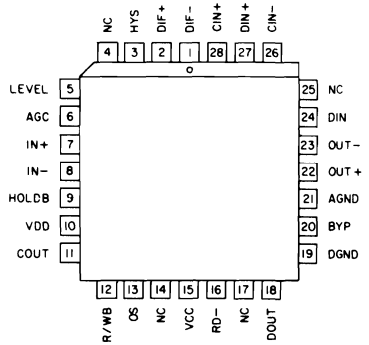
Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

PIN CONNECTIONS

24-Pin PDIP



28-Lead PLCC



PIN DESCRIPTION

PIN NAME	DESCRIPTION
VCC	5 volt power supply
VDD	12 volt power supply
AGND, DGND	Analog and Digital ground pins
R/WB	TTL compatible read/write control pin
IN+, IN-	Analog signal input pins
OUT+, OUT-	AGC Amplifier output pins
BYP	The AGC timing capacitor is tied between this pin and AGND
HOLDB	TTL compatible pin that holds the AGC gain when pulled low
AGC	Reference input voltage level for the AGC circuit
DIN+, DIN-	Analog input to the hysteresis comparator

PIN NAME	DESCRIPTION
HYS	Hysteresis level setting input to the hysteresis comparator
LEVEL	Provides rectified signal level for input to the hysteresis comparator
DOUT	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	Analog input to the differentiator
DIF+, DIF-	Pins for external differentiating network
COUT	Buffered test point for monitoring the clock input to the flip-flop
OS	Connection for read output pulse width setting capacitor
RD	TTL compatible read output

ABSOLUTE MAXIMUM RATINGS*

5V Supply Voltage, VCC 6V
12V Supply Voltage, VDD 14V
Storage Temperature ..... -65° to 150°C
Lead Temperature ..... 260°C
R/$\overline{W}$, IN+, IN-, HOLS ..... -0.3V to VCC + 0.3V
RD ..... -0.3 to VCC + 0.3V or + 12mA
All others ..... -0.3V to VCC + 0.3V

*Operation above these rating may cause permanent damage to device.

R/WB	HOLDB	MODE
1	1	READ — Read amp on, AGC active, Digital section active
1	0	HOLD — Read amp on, AGC gain held constant, Digital section active
0	X	WRITE — AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

ELECTRICAL CHARACTERISTICS: Unless otherwise specified 4.5V ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25C ≤ Tj ≤ 135C

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY					
ICC—VCC Supply Current	Outputs unloaded	—	—	14	mA
IDD—VDD Supply Current	Outputs unloaded	—	—	70	mA
Pd—Power Dissipation	Outputs unloaded, Tj = 135C	—	—	730	mW
LOGIC SIGNALS					
VIL—Input Low Voltage	—	-0.3	—	0.8	V
VIH—Input High Voltage	—	2.0	—	—	V
IIL—Input Low Current	VIL = 0.4V	0.0	—	-0.4	mA
IIH—Input High Current	VIL = 2.4V	—	—	100	μA
VOL—Output Low Voltage	IOL = 4.0mA	—	—	0.4	V
VOH—Output High Voltage	IOH = -400μA	2.4	—	—	V

ELECTRICAL CHARACTERISTICS: (CONTINUED) Unless otherwise specified 4.5V ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25C ≤ Tj ≤ 135C

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
MODE CONTROL					
Read to Write Transition Time	—	—	—	1.0	μS
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2	—	3.0	μS
Read to Hold Transition Time	—	—	—	1.0	μS
WRITE MODE					
Common Mode Input Impedance (both sides)	R/WB Pin = low	—	250	—	Ω
READ MODE					
AGC Amplifier Unless otherwise specified IN+ and IN- are AC coupled, OUT+ and OUT- are loaded differentially with 600Ω and each side is loaded with >10pf to GND, a 2000pf capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.					
Differential Input Resistance	V(IN+ --IN-) = 100 mVpp @ 2.5MHz		5K		Ω
Differential Input Capacitance	V(IN+ --IN-) = 100 mVpp @ 2.5MHz			10	pF
Common Mode Input Impedance (both sides)	R/WB pin high R/WB pin low		1.8 0.25		KΩ KΩ
Gain Range	1.0Vpp≤V(OUT+ --OUT-) = 2.5 Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/√Hz
Bandwidth	Gain set to maximum -3dB point	30			MHz
Maximum Output Voltage Swing		3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND	±3.2			mA
Output Resistance		13		32	Ω
Ouput Capacitance				15	pF
(Din+ --DIN-) Input Voltage Swing VS AGC Input Level	30mVpp ≤V(IN+ --IN-) ≤550mVpp 0.5Vpp ≤V(DIN+ --DIN-) ≤1.5Vpp	0.37		0.56	Vpp/V
(Din+ --DIN-) Input Voltage Swing Variation	30mVpp V(IN+ --IN-) ≤550mVpp AGC Fixed, over supply & temp.			8	%
Gain Decay time (Td)	Vin = 300mVpp-->150mVpp at 2.5MHz, Vout to 90% of final value Fig. 1a		50		μS
Gain Attack Time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400mVpp @ 2.5MHz. Fig. 1B		4		μS
Fast AGC Capacitor Charge Current	V(DIN+ = DIN-) = 1.6V V(AGC) = 2.2V	1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ --DIN-) = 1.6V Vary V(AGC) until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	V(DIN+ --DIN-) V(DIN+ --DIN-) Final		1.25		
AGC Capacitor Discharge Current	V(DIN+ --DIN-) = 0.0V Read Mode Hold Mode	 -0.2	4.5	 +0.2	 μA μA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100mVpp @ 5MHz, gain at max.	40			dB
PSRR (Input Referred)	VCC or VDD = 100mVpp @ 5MHz, gain at max	30			dB
HYSTERESIS COMPARATOR					
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ --DIN-) = 100mVpp@ 2.5MHz	5		11	KΩ
Differential Input Capacitance	V(DIN+ --DIN-) = 100mVpp@ 2.5MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		KΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5KΩ across DIN+, DIN-			10	mV
Peak Hysteresis Voltage vs HYS pin voltage (input referred)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16		0.25	V/V V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	μA
Level Pin Output Voltage vs V(DIN+ --DIN-)	0.6 < |V (DIN+ --DIN-)| < 1.3Vpp 10KΩ from LEVEL pin to GND	1.5		2.5	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5mA		180		Ω
DOUT Pin Output Low Voltage	0.0≤IOL≤0.5mA	VDD-4.0		VDD-2.8	V
DOUT Pin Output High Voltage	0.0≤IOH≤0.5mA	VDD-2.5		VDD-1.8	V

ACTIVE DIFFERENTIATOR

PARAMETER	TEST CONDITIONS	MIN.	NOM.	MAX.	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ --CIN-) = 100mVpp @ 2.5MHz	5.8		11.0	KΩ
Differential Input Capacitance	V(CIN+ --CIN-) = 100mVpp @ 2.5MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		KΩ
Voltage Gain From CIN+/- to DIF +/-	R(DIF+ to DIF-) = 2 KΩ	1.7		2.2	V/V
DIF+ to DIF- Pin current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF = AC Coupled			10.0	mV
COUT Pin Ouput Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD-3.0		V
COUT Pin Ouput Pulse Voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		nS

OUTPUT DATA CHARACTERISTICS (REF. FIG. 2) Unless otherwise specified V(CIN+ - CIN-) = V(DIN+ - DIN-) = 1.0Vpp AC coupled since wave at 2.5MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65pF, V (Hys) = 1.8DC, a 60pF capacitor is connected between OS and VCC, RD- is loaded with a 4KΩ resistor to VCC and a 10pF capacitor to GND.

D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ - DIF-) reaching a peak	0	—	—	nS
Propagation Delay (Td3)	—	—	—	110	nS
Output Data Pulse Width Variation	Td5 = 670 Cos, 50 pF ≤ Cos ≤ 200 pF	—	—	±15	%
Logic Skew Td3—Td4	—	—	—	3	nS
Output Rise Time	VOH = 2.4V	—	—	14	nS
Output Fall Time	VOL = 0.4V	—	—	18	nS

AGC TIMING DIAGRAM

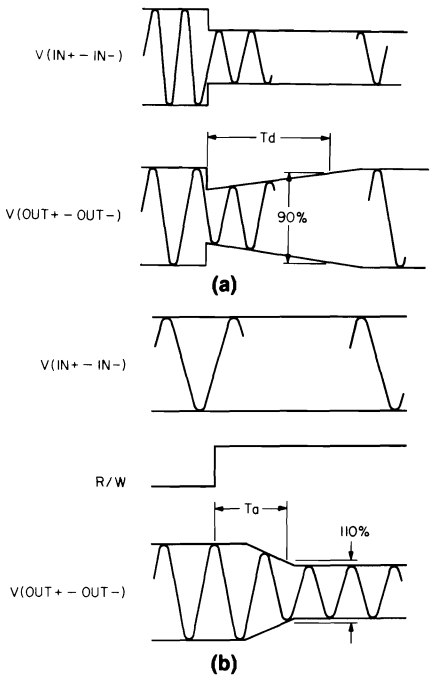


Fig. 1

TIMING DIAGRAM

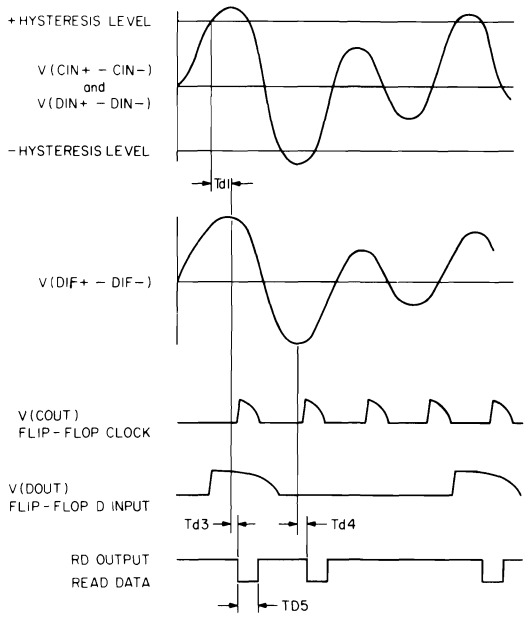
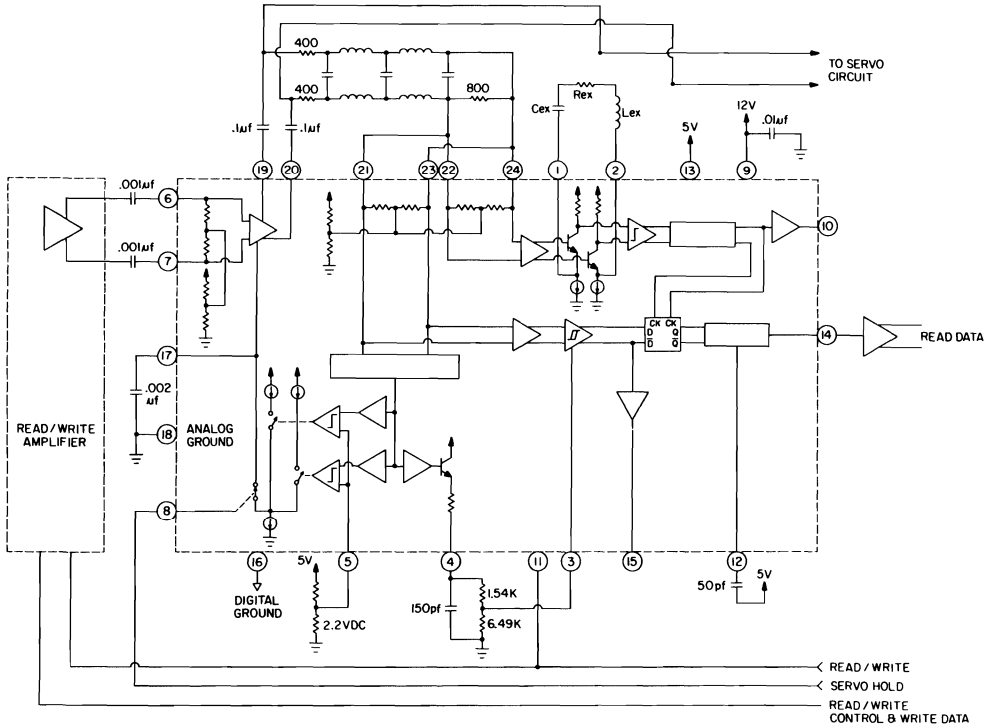


Fig. 2

TYPICAL READ/WRITE ELECTRONICS SET UP

(component values, where given, are in a 5MB/sec system)



NOTE: Circuit traces for the 12V bypass capacitor and the AGC hold capacitor should be as short as possible with both capacitors returned to the Analog Ground pin.

Fig. 3

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-541FN	28 Lead PLCC
CS-541N	24 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-570

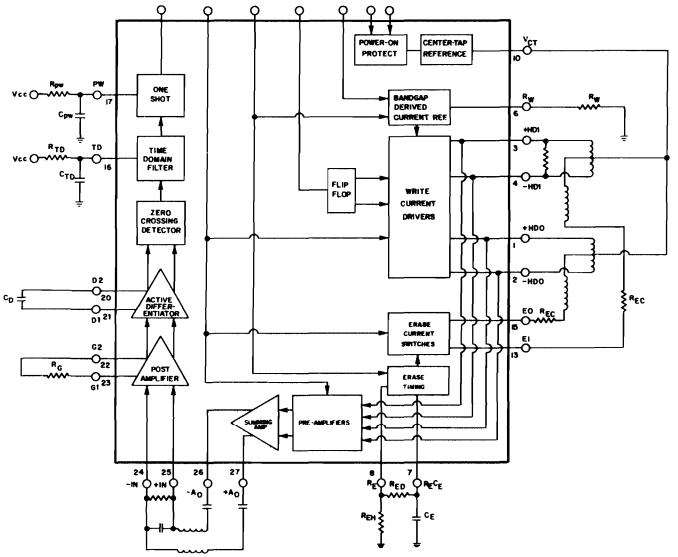
2-CHANNEL FLOPPY DISK READ/WRITE CIRCUIT

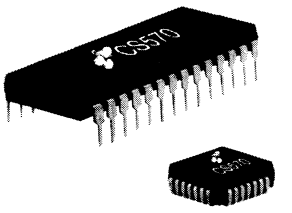
DESCRIPTION

The CS-570 is an integrated circuit which performs the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The write data circuitry includes switching differential current drivers and erase head drive is with programmable delay and hold times. The read data circuitry includes low noise amplifiers for each channel as well as a programmable gain stage and necessary equalization and filtering capability using external passive components. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility. The circuit operates on +12 volt and +5 volt power supplies and is available in 28 pin plastic DIP and QUAD packages.

The CS-570 combined with the CS-279 provides a complete two-chip floppy disk drive control.

BLOCK DIAGRAM

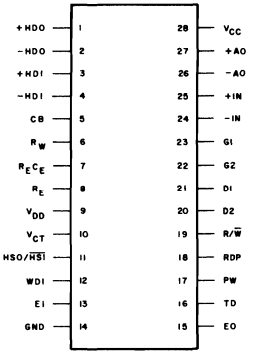




FEATURES:

- Single chip read/write amplifier and read data processing function.
- Compatible with 8", 5¼", and 3½" drives.
- Internal write and erase current sources, externally set.
- Internal center tap voltage source.
- Contol signal are TTL compatible.
- Schmitt trigger inputs for higher noise immunity on bussed control signals.
- TTL selectable write current boost.
- Operates on +12 volt and +5 volt power supplies.
- High gain, low noise, low peak shift (0.3% Typ) read processing circuits.

PIN CONNECTIONS



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
(401) 885-3600 Telefax (401) 885-5786 Telex WUI 6817157

Circuit Operation

WRITE MODE CIRCUITRY

In Write Mode (R/$\overline{W}$ low), the circuit provides controlled write and erase currents to either of two magnetic heads. The Write-Erase circuitry consists of two differential Write Current Drivers, a Center Tap Voltage Reference, two Erase Current Switches and control circuits for head selection and erase timing.

Write current is toggled between opposing sides of the head on each negative transition of the Write Data Input (WDI) and is set externally by a single resistor, R_W, connected between the R_W terminal and ground. Since driver output impedance is large, proper damping resistors must be provided across each head. A signal at the CB terminal provides write current boost.

Erase current is also set externally through resistors R_{EC} connected in series with each erase coil. Erase can be activated by, but delayed from, selection of the write mode, and is held active after mode deselection. The turn-on delay is determined by the charging of C_E through R_{ED}, while the hold time is determined by the discharge of C_E through the series combination of R_{ED} and REH (see connection diagram). The R_EC_E node may be driven directly by a logic gate, with external resistors per fig. 4, if the erase period is to be controlled separately from the write mode selection. For applications where no delays are required, C_E is omitted.

The Center Tap Voltage Reference supplies both write and erase currents. A Power Turn-On protection circuit prevents undesired writing or erasure by holding the voltage reference off until the supply voltages are within their operating ranges.

READ MODE CIRCUITRY

In the Read Mode (R/$\overline{W}$ high), the circuit performs the functions of amplifying and detecting the selected head output pulses which correspond to magnetic transitions in the media. The Read circuitry consists of two differential Preamplifiers, a Summing Amplifier, a Postamplifier, an Active Differentiator, a Zero-Crossing Detector, a Time Domain Filter, and an Output One-Shot.

The selected Preamplifier drives the Summing Amplifier whose outputs are AC coupled to the Postamplifier through an external filter network. The Postamplifier adjusts signal amplitudes prior to application of signals to the Active Differentiator. Postamplifier gain is set as required by connecting a resisitor across the gain terminals, G1 and G2. If desired, an additional frequency/phase compensation network may also be connected across these gain terminals.

The Differentiator, driven by the Postamplifier, provides zero-crossing output voltages in response to input signal peaks. Differentiator response characteristics are set by an external capacitor or more complex series network connected between the D1 and D2 terminals.

The Zero-Crossing Detector provides a unipolar output for each positive or negative zero-crossing of the Differentiator output. To enhance signal peak detection, the Time Domain Filter inhibits the detection of zero-crossings if they are not sufficiently separated in time. The filter period is set by an external RC network connected to the TD pin.

The Time Domain Filter drives the output One-Shot which generates uniform output data pulses. The pulse width is set by an external RC network connected to the PW pin. The Output One-Shot is inhibited while in the Write Mode.

ABSOLUTE MAXIMUM RATINGS

5V Supply Voltage, V_{CC} 7V
12V Supply Voltage, V_{DD} 14V
Storage Temperature ..... -65°C to +130°C
Ambient Operating Temperature ..... 0°C to +70°C
Junction Operating Temperature ..... 0°C to +130°C
Logic Input Voltage ..... $-0.5V_{dc}$ to $7.0V_{dc}$
Lead Temperature (soldering, 10sec) ..... 260°C
Power Dissipation 800mW

ELECTRICAL SPECIFICATIONS: Unless otherwise stated: $4.75V \leq V_{CC} \leq 5.25V$; $11.4V \leq V_{DD} \leq 12.6V$; $0°C \leq T_A \leq 70°C$; $R_W = 430\Omega$; $R_{ED} = 62k\Omega$; $C_E = 0.012\ \mu F$; $R_{EH} = 62k\Omega$; $R_{EC} = 220\Omega$

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNITS
POWER SUPPLY CURRENTS				
I_{CC} — 5V Supply Current	Read Mode	—	35	mA
	Write Mode	—	38	mA
I_{DD} — 12V Supply Current	Read Mode	—	26	mA
	Write Mode (excluding Write & Erase currents)	—	24	mA
LOGIC SIGNALS — READ/WRITE (R/W), CURRENT BOOST (CB)				
Input Low Voltage (V_{IL})		—	0.8	V
Input Low Current (I_{IL})	$V_{IL} = 0.4V$	—	-0.4	mA
Input High Voltage (V_{IH})		2.0	—	V
Input High Current (I_{IH})	$V_{IH} = 2.4V$	—	20	μ

ELECTRICAL SPECIFICATIONS (CONTINUED): Unless otherwise stated:4.75V $\leq V_{CC} \leq$5.25V; 11.4V $\leq V_{DD} \leq$12.6V; 0°C $\leq T_A \leq$70°C; R_W = 430Ω; R_{ED} = 62kΩ; C_E =0.012 μF; R_{EH} = 62kΩ; R_{EC} = 220Ω

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNITS
LOGIC SIGNALS — WRITE DATA INPUT (WDI), HEAD SELECT (HS0/HS1)				
Threshhold Voltage, V_T + Positive — going		1.4	1.9	V
Threshold Voltage, V_T- Negative — going		0.6	1.1	V
Hysteresis, V_T + to V_T-		0.4	—	V
Input High Current, I_{IH}	V_{IH} = 2.4V	—	20	μA
Input Low Current, I_{IL}	V_{IL} =0.4V	—	-0.4	mA
CENTER TAP VOLTAGE REFERENCE				
Output Voltage (V_{CT})	I_{WC} + I_E = 3mA to 60mA	V_{DD}-1.5	V_{DD}-.5	V
V_{CC} Turn-Off Threshold	(See Note 1)	4.0	—	V
V_{DD} Turn-Off Threshold	(See Note 1)	9.6	—	V
V_{CT} Disabled Voltage		—	1.0	V
ERASE OUTPUTS (E1, E0)				
Unselected Head Leakage	V_{E0}, V_{E1} = 12.6V	—	100	μA
Output on Voltage (V_{E1}, V_{E0})	I_E = 50mA	—	0.5	V
WRITE CURRENT				
Unselected Head Leakage	V_{E1}, V_{E0} = 12.6V	—	25	μ
Write Current Range	R_W = 820Ω to 180Ω	3	10	mA
Current Reference Accuracy	I_{WC} = 2.3/RW V_{CB} (current boost) =0.5V	-5	+5	%
Write Current Unbalance	I_{WC} = 3mA to 10mA	—	1.0	%
Differential Head Voltage Swing	$\Delta I_{WC} \leq$5%	12.8	—	Vpk
Current Boost	V_{CB} = 2.4V	1.25 I_{WC}	1.35 I_{WC}	—
ERASE TIMING				
Erase Delay Range	R_{ED} = 39kΩ to 82kΩ; C_E = 0.0015 μF to 0.043 μF	0.1	1.0	msec
Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100\%$	$T_{ED} = 0.69 R_{ED} C_E$ R_{ED} = 39kΩ to 82kΩ; C_E = 0.0015 μF to 0.043 μF	-15	+15	%
Erase Hold Range	$R_{EH} + R_{ED}$ = 78kΩ to 164kΩ; C_E = 0.0015 MF to 0.043 MF	0.2	2.0	msec
Erase Hold Accuracy $\frac{\Delta T_{EH}}{T_{EH}} \times 100\%$	T_{EH} = 0.69 (R_{EH} + R_{ED}) C_E R_{EH} = R_{EH} = 78kΩ to 164kΩ; C_E = 0.0015 μF to 0.043 μF	-15	+15	%

ELECTRICAL SPECIFICATIONS: Unless otherwise stated: V_{IN} (Preamplifier) = 10mVp-p sine wave, dc coupled to center tap. (See figure 1). Summing Amplifier Load =2kΩ line-line, ac coupled. V_{IN} (Postamplifier) =0.2Vp-p sine wave, ac coupled; R_G =open; Data Pulse Load = 1kΩ to Vcc; C_D = 240pF; C_{TD} = 100pF; R_{TD} =7.5kΩ; C_{PW} = 47 pF; R_{PW} = 7.5kΩ.

PREAMPLIFIER — SUMMING AMPLIFIER

Differential Voltage Gain	Freq. = 250kHz	85	115	V/V
Bandwidth (-3 dB)		3	—	MHz
Gain Flatness	Freq. = dc to 1.5MHz	—	±1.0	dB
Differential Input Impedance	Freq. = 250kHz	20	—	kΩ
Max. Differential Output Voltage Swing	V_{IN} = 250kHz sine wave, THD $\leq$ 5%	2.5	—	Vp-p
Small Signal Differential Output Resistance	$I_O \leq$ 1.0mAp-p	—	75	Ω

ELECTRICAL SPECIFICATIONS (CONTINUED)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNITS
PREAMPLIFIER — SUMMING AMPLIFIER (CONTINUED)				
Common Mode Rejection Ratio	V_{IN} = 300mVp-p @ 500kHz. Inputs shorted.	50	—	dB
Power Supply Rejection Ratio	ΔV_{DD} = 300mVp-p @ 500kHz Inputs shorted to V_{CT}.	50	—	dB
Channel Isolation	Unselected Channel V_{IN} = 100mVp-p 500kHz. Selected channel input connected to V_{CT}.	40	—	dB
Equivalent Input Noise	Power BW = 10kHz to 1MHz Inputs shorted to V_{CT}.	—	10	μVrms
Center Tap Voltage, V_{CT}		1.5 (typ)		V
POSTAMPLIFIER — ACTIVE DIFFERENTIATOR				
Ao, Differential Voltage Gain +IN, -IN to D1, D2	Freq. = 250kHz (See Figure 2)	8.5	11.5	V/V
Bandwidth(-3 dB +IN, -IN to D1, D2	C_D = 0.1μF, R_D = 2.5kΩ	3	—	MHz
Gain Flatness +IN, -IN to D1, D2	Freq. = dc to 1.5 MHz C_D = 0.1 μF, R_D = 2.5kΩ	—	±1.0	dB
Max. Differential Output Voltage Swing	V_{IN} = 250kHz sine wave, ac coupled. ≤5% THD in voltage across C_D. (See Figure 2)	5.0	—	Vp-p
Max. Differential Input Voltage	V_{IN} = 250kHz sine wave, ac coupled. ≤5% THD in voltage across C_D. R_G = 1.5kΩ	2.5	—	Vp-p
Differential Input Impedance		10	—	kΩ
Gain Control Accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G/(8 \times 10^3 + R_G$ R_G = 2kΩ	-25	+25	%
Threshold Differential Input Voltage. (See Note 2)	Min. differential input voltage at post amp that results in a change of state at RDP. V_{IN} = 250kHz square wave, C_D = 0.1 μF, R_D = 500Ω, T_R, $T_F \leq$ 0.2 μsec. No overshoot; Data Pulse from each V_{IN} transition. (See Figure 3)	—	3.7	mVp-p
Peak Differentiator Network Current		1.0	—	mA
TIME DOMAIN FILTER				
Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	$T_{TD} = 0.58\ R_{TD} \times (C_{TD} + 10^{11}) + 50$nsec, R_{TD} = 5kΩ to 10kΩ, $C_{TD} \geq$ 56pF V_{IN} = 50m Vpp @ 250kHz square wave, T_R, $T_F \leq$20 nsec, ac coupled. Delay measured from 50% input amplitude to 1.5V Data Pulse.	-15	+15	%
Delay Range	$T_{TD} = 0.58\ R_{TD} \times (C_{TD} + 10^{11}) + 50$ nsec R_{TD} = 5kΩ to 10kΩ C_{TD} = 56pF to 240pF	240	2370	ns
DATA PULSE				
Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	$T_{PW} = 0.58\ R_{PW} \times (C_{PW} + 8 \times 10^{12}) + 20$nsec R_{PW} = 5kΩ to 10kΩ C_{PW} = ≥36pF width measured at 1.5V amplitudes	-20	+20	%
Active Level Output Voltage	I_{OH} = 400μA	2.7		V
Inactive Level Output Leakage	I_{OL} = 4mA	—	0.5	V
Pulse Width	$T_{PW} = 0.58\ R_{PW} \times (C_{PW} + 8 \times 10^{12}) + 20$nsec R_{PW} = 5kΩ to 10kΩ C_{PW} = 36pF to 200 pF	145	1225	nS

NOTES:
1. Voltage below which center tap voltage reference is disabled.
2. Threshold Differential input Voltage can be related to peak shift by the following formula:

$$\text{Peak Shift} = \frac{3.7\text{mV}}{\mu\text{Vin}} \times 100\%$$

where Vin = peak to peak input voltage at post amplifier.
Note that this formula demonstrates an inverse relationship between the input amplitude and the Peak Shift.

TEST SCHEMATICS

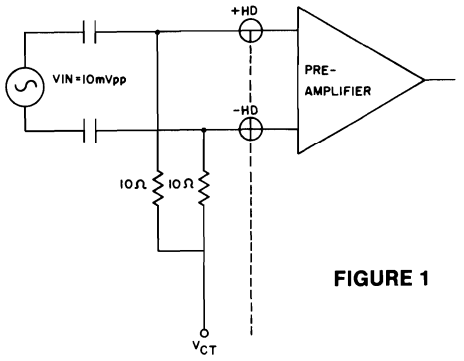


FIGURE 1

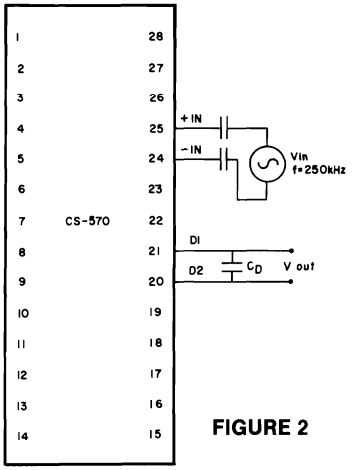


FIGURE 2

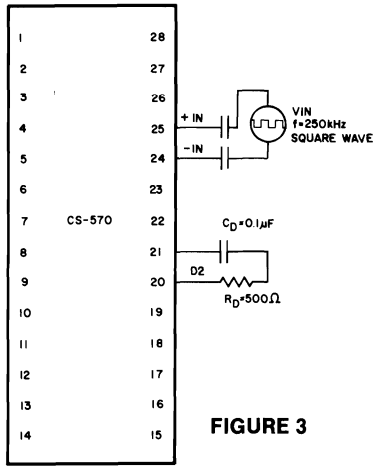


FIGURE 3

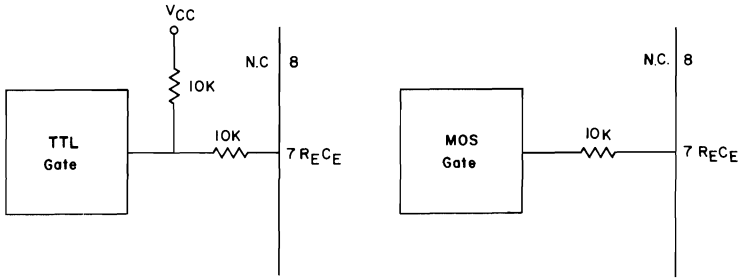


FIGURE 4

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-570FN	28 Lead PLCC
CS-570N	28 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

HIGH EFFICIENCY PRECISION SERVO CONTROLLER

CS-2017™

DESCRIPTION

The CS-2017 is designed to reduce the power consumption and space required for closed-loop control of voice coil actuator motors in disc head positioning servos and other precision servos. The CS-2017 includes the current sense amplifier, bridge output power drive and the error amplifier

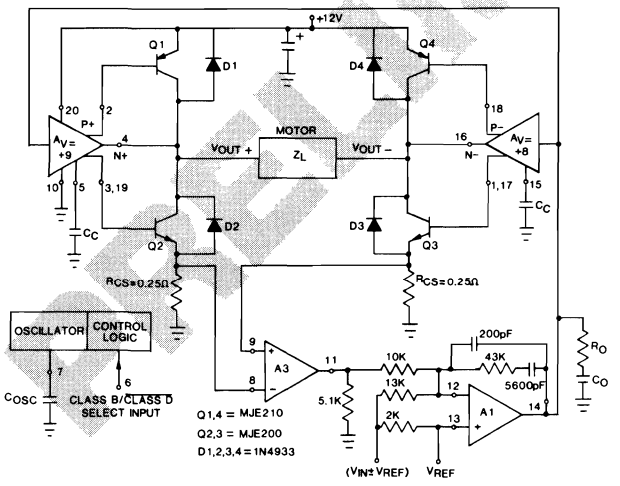
The CS-2017 saves power by using a Class D (chopper) mode output drive during the high current "seek" operation. System dissipation is reduced by a factor of three providing higher reliability and easier heat management. During the lower current "tracking" operation, the amplifier switches to conventional Class B analog mode for noise-free data retrieval. A logic input selects the operation mode the bridge output stage is designed for minimum saturation voltage allowing efficient operation with single supply voltage from 4.5 to 20V.

A low offset differential amplifier senses the output current in the bridge ground return and provides a proportional voltage added to the externally-generated common-mode reference voltage. This closes the loop and makes the servo amplifier a voltage in, current out system.

The CS-2017 contains all of the control circuitry required for the application. This allows the circuit designer to select power transistors and catch diodes to meet the output voltage and current specifications of almost any application. External transistors also allow greater flexibility for thermal and space management.

The CS-2017 is available in both 20L PDIP and 20L PLCC.

BLOCK DIAGRAM



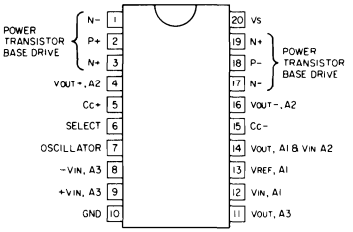
FEATURES:

- Low Saturation Voltage
- Precision Current Sense Amplifier
- Efficient Class D Switch Mode
- Linear Class B Track Mode
- Single Supply Operation 4.5 to 20V

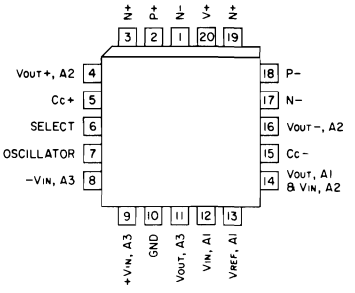
APPLICATIONS:

- Winchester Disc Head Positioning Servo
- 3.5" Disc Drive Servo
- Galvo Motors
- Robotics
- DC Motor Controls

PIN CONNECTIONS
Dip Package
(Top View)



PLCC Package



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

V_S Supply Voltage 20V
V_{IN} Input Voltage Range (any logic pin) ..... -0.3V to V_S
Sense Amp Input Voltage Range ..... -1.5V to V_S
Sense Amp Differential Input Voltage Range .... ±5V
T_J Junction Temperature ..... 150°C

T_A Operating Temperature Range ..... -25°C to +85°C
Lead Temperature
(soldering, 10 seconds) ..... 300°C
T_{ST} Storage Temperature ..... -65°C to +150°C
P_D Power Dissipation (T_A-25°C) 1.25W

ELECTRICAL CHARACTERISTICS: T_j=T_A=25°C (Note 7)

PARAMETER	MODE	VOLTS			MIN.	TYP.	MAX.	UNITS
		V_S	V_{REF}	V_{IN}				
System, Closed-Loop								
K Gain Constant, I_{OUT}/V_{IN}, I_{OUT}=±100mA	B	12	5	Note 1	0.85	1	1.15	A/V
I_{OS} Output Offset Current	B	12	5	5	-35	5	35	mA
	B	12	8	8	-40	5	40	mA
	B	12	2	2	-40	5	40	mA
	B	4.5	2	2	-40	5	40	mA
	B	20	2	2	-40	5	40	mA
	B	20	16	16	-40	5	40	mA
	Standby	12	5	5	-2	0	2	mA
I_Q Quiescent Supply Current	B	12	5	Open		25	50	mA
	D	12	5	Open		20	50	mA
	Standby	12	5	Open		12	25	mA
	B	20	5	Open		40	100	mA
	D	20	5	Open		25	100	mA
	Standby	20	5	Open		20	50	mA
I_{OUT} Output Drive Current	B	12	5	Note 2	15	30		mA
	D	12	5	Note 2	45	60		mA
R_{OUT} Standby Output Resistance (Note 4)	Standby	12	5	Open	1	4		kΩ
I_{IH} Select High Current (20V)	B	12	5	5		0	10	μA
I_{IL} Select Low Current (0V)	D	12	5	5		-10	-200	μA
I_{IL} Oscillator Low Current (0.4V)	Standby	12	5	5		-100	-400	μA
I_{BREF} Reference Voltage Bias Current	Standby	12	5	Open	0.2	0.6	1	mA
Current Sense Amplifier								
A3 Current Sense Amp Gain, Pin 9=±400mV	Standby	12	5	Open	3.6	4	4.4	V/V
V_{OSO} Current Sense Amp Output Offset	Standby	12	5	Open	-20	5	20	mV
	Standby	12	8	Open	-30	5	30	mV
	Standby	12	2	Open	-30	5	30	mV
	Standby	4.5	2	Open	-30	5	30	mV
	Standby	20	2	Open	-30	5	30	mV
	Standby	20	16	Open	-30	5	30	mV
RVRR Reference Voltage Rejection Ratio	Standby	20	Note 5	Open	50	75		dB
PSRR Power Supply Rejection Ratio	Standby	Note 6	2	Open	50	75		dB
CMRR Common-Mode Rejection Ratio Pin 8=Pin 9=±500mV	Standby	12	5	Open	50	75		dB
I_{OUT} Output Source Current	Standby	12	5	Open	+5	+10		mA
I_B Input Current	Standby	12	5	Open	0.2	0.6	1	mA

ELECTRICAL CHARACTERISTICS: (Continued) $T_j=T_A=25°C$ (Note 7)

PARAMETER	MODE	VOLTS			MIN.	TYP.	MAX.	UNITS
		V_S	V_{REF}	V_{IN}				
Error Amplifier								
V_{OS} Offset Voltage	B	12	5	Open	-10	2	10	mV
	B	12	8	Open	-10	2	10	mV
	B	12	2	Open	-10	2	10	mV
	B	4.5	2	Open	-10	2	10	mV
	B	20	2	Open	-10	2	10	mV
	B	20	16	Open	-10	2	10	mV
RVRR Reference Voltage Rejection Ratio	B	20	Note 5	Open	50	75		dB
PSRR Power Supply Rejection Ratio	B	Note 6	2	Open	50	75		dB
I_{OUT} Output Current	B	12	5	Open	±5	±20		mA
Driver Amplifier								
A2 Driver Amp Gain, I_{OUT}=±750mA	B	12	5	Note 1	10	17	20	V/V
f_{osc} Switching Frequency, I_{OUT}=±500mA	D	12	5	Note 1	20	30	40	kHz
Duty Cycle, I_{OUT}=±500mA	D	12	5	Note 1	35	45	55	%
V_S Supply Voltage Operating Range	Guaranteed by above tests				4.5	12	20	V
V_{REF} Reference Operating Range	Guaranteed by above tests				2	5	V_S-4	V

Note 1: V_{IN} is adjusted to set I_{OUT}.

Note 2: V_{IN}=2V for $I_{OUT} < 0A$, and V_{IN}=8V for $I_{OUT} > 0A$.

Note 3: $2.5V < V_{REF} < 16V$.

Note 4: $V_{OUT}=V_S/2$.

Note 5: $2V < V_{REF} < 16V$.

Note 6: $4.5V < V_S < 20V$.

Note 7: Mode B is forced with pin 6=2.0V and pin 7 open. Mode D is forced with pin 6=0.6V and pin 7 open. Standby is forced with pin 6=0.6V and pin 7=0.4V.

ORDERING INFORMATION

Part Number	Temp. Range	Description
CS-2017N	-25 to +85°C	20 Lead PDIP
CS-2017FN	-25 to +85°C	20 Lead PLCC

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-593C
CS-594C
CS-595C

PULSE WIDTH MODULATOR CONTROL CIRCUIT
WITH OUTPUT CONTROL FOR S-E or P-P OPERATION

DESCRIPTION

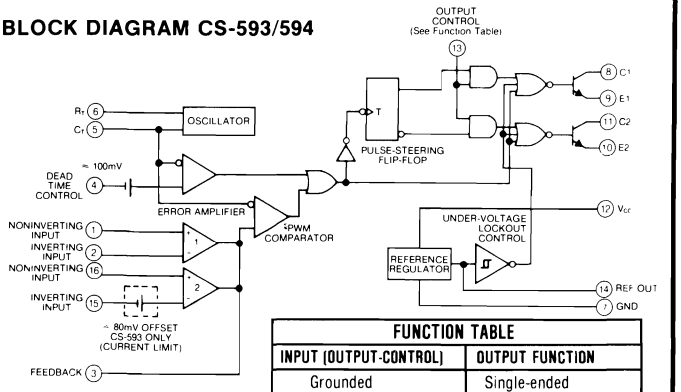
CS-593, CS-594 and CS-595 incorporate all the functions required in the construction of a PWM power supply control circuit. The CS-593 contains an on-chip 5V precision reference, an error amplifier, a current-limit sense amplifier, adjustable oscillator, dead-time control comparator, pulse steering flip-flop, and output control circuitry. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Single-ended or push-pull output operation may be selected by means of the output control function.

The architecture of the CS-593 prohibits the possibility of either output being pulsed twice during push-pull operation. The internal error amplifier exhibits a common-mode voltage range from 0.3 volt to Vcc -2 volts. The current limit sense amplifier has an 80 millivolt offset in series with the inverting input, eliminating the need for external components. The dead time comparator has a fixed offset that provides approximately 5% dead time unless externally altered. The on-chip oscillator may be by-passed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common CS-593 circuitry and provide a sawtooth input for associated control circuitry in synchronous multiple-rail power supplies.

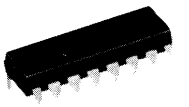
The CS-594 provides the same functions as the CS-593, except for the current-limit amplifier. The CS-594 contains two error amplifiers for design flexibility. Both of these internal amplifiers exhibit a common-mode voltage range of 0.3 volt to Vcc -2 volts. The rest of the functions are identical in both devices.

The CS-595 provides the same functions found in the CS-594, but in addition contains an on-chip 39-volt zener diode for applications where Vcc is greater than 40 volts. The CS-595 also incorporates an output steering control that overrides the internal control of the pulse-steering flip-flop.

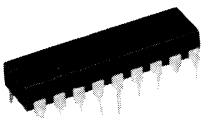
BLOCK DIAGRAM CS-593/594



FUNCTION TABLE	
INPUT (OUTPUT-CONTROL)	**OUTPUT FUNCTION**
Grounded	Single-ended or parallel output
At V_{ref}	Normal push-pull operation



CS-593
CS-594

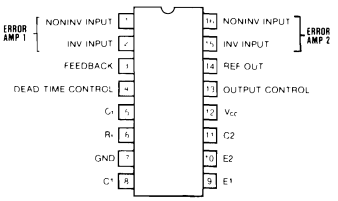


CS-595

FEATURES:

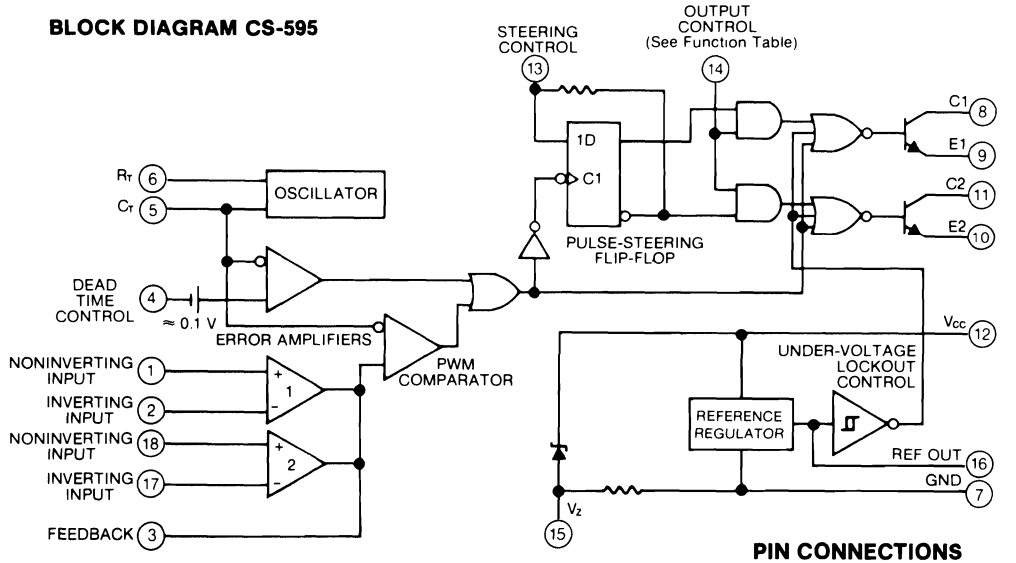
- Dual 200mA Outputs
- High Performance Current Limit (CS-593)
- Two Error Amplifiers for Design Flexibility (CS-594/595)
- Adjustable Dead-time
- Under Voltage Lockout
- Double Pulse Inhibit
- Stable 5V ±1% Reference
- External Control of Output Steering (CS-595)
- Output Control for Single-Ended or Push-pull Operation
- On-chip 39V Zener for Operation at Vcc > 40V (CS-595)

PIN CONNECTIONS
CS-593/594

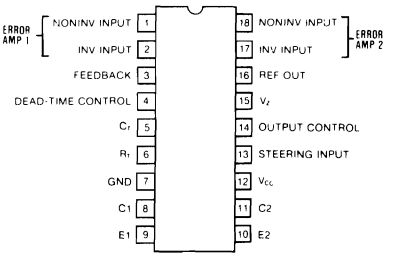


(TOP VIEW)

BLOCK DIAGRAM CS-595



PIN CONNECTIONS
CS-595



FUNCTION TABLE			
INPUTS			
OUTPUT CONTROL	STEERING CONTROL	OUTPUT FUNCTION	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Open	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Open	Push-pull operation	0.5
At V_{ref}	V1 <0.4 V	Single-ended P.W.M. at Q1 only	1
At V_{ref}	V1 >2.4V	Single-ended P.W.M. at Q2 only	1

CIRCUIT OPERATION

The CS-593/4/5 are fixed-frequency pulse width modulation control circuits, incorporating the primary building blocks required for the control of a switching power supply. An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of ouput pulse width.

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the ouput control grounded, and 48% with it connected to the reference line. Additional dead-time may be imposed on the output by setting the dead-time control input to a fixed voltage, ranging between 0 to 3.3V

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead-time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from 0.3 V to (V_{cc} -2V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The CS-593/4/5 has an internal 5 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1% with a thermal drift of less than 50 mV over the operating temperature range.

The CS-595 contains an on-chip 39 volt zener diode for high voltage applications where V_{cc} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse steering flip-flop. (Refer to the function table).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 41V
Collector Output Voltage 41V
Collector Output Current ..... 250 mA
Amplifier Input Voltages ..... V_{CC} +0.3 V
Power Dissipation, $T_A \leq 25°C$ 1000mW
Operating Temperature ..... 0 to 70°C
Storage Temperature ..... -65 to +150°C

RECOMMENDED OPERATING CONDITIONS:

Supply Voltage, V_{cc} ..... 7 to 40V
Collector Output Voltage 40V
Collector Output Current 200mA
Error Amplifier Input ..... 0.3 to V_{cc} -2V
Current Limit Amplifier Input (CS-593) ..... 0.3V to V_{cc} -6V
Current Into Feedback Terminal ..... 0.3 mA
Timing Resistor, R_T ..... 1.8 to 500 KΩ
Timing Capacitor, C_T ..... 0.47 to 10,000 nF
Oscillator Frequency ..... 1 to 300 KHz

ELECTRICAL CHARACTERISTICS (Over operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz, unless otherwise noted.)

PARAMETER		TEST CONDITIONS		MIN.	TYP	MAX	UNIT
Output voltage (V_{ref})		I_O = 1 mA, T_A = 25°C		4.95	5	5.05	V
Input regulation		V_{CC} = 7 V to 40 V, T_A = 25°C			2	25	mV
Output regulation		I_O = 1 to 10mA, T_A = 25°C			14	35	mV
Output voltage change with temperature		T_A = 0°C to 70°C			0.2	1	%
Short-circuit output current†		V_{ref} = 0		10	35	50	mA
Oscillator Section							
Frequency		C_T = 0.01 μF, R_T 12 kΩ			10		kHz
Standard deviation of frequency		All values of V_{CC}, C_T, R_T, T_A constant			10		%
Frequency change with voltage		V_{CC} = 7V to 40V, T_A = 25°C			0.1		%
Frequency change with temperature		C_T = 0.01 μF, R_T = 12 kΩ, T_A = 0°C to 70°C				2	%
Dead-time Control-Section (see figure 1)							
Input bias current (pin 4)		V_I = 0 to 5.25V			-2	-10	μA
Maximum duty cycle, each output		V_I (pin 4) = 0		45			%
Input threshold voltage (pin 4)		Zero duty cycle			3	3.3	V
		Maximum duty cycle		0			
Amplifier Sections							
Input offset voltage	Error	V_O (pin 3) = 2.5V			2	10	mV
	Current-limit		CS-593		80		
Input offset current		V_O (pin 3) = 2.5V			25	250	nA
Input bias current		V_O (pin 3) = 2.5V			0.2	1	μA
Common-mode input voltage range	Error	V_{CC} = 7V to 40V		0.3 to V_{CC}-2			V
	Current-limit		CS-593	0.3 to V_{cc}-6			
Open-loop voltage amplification	Error	ΔV_O = 3V, V_O = 0.5 to 3.5V		70	95		dB
	Current-limit		CS-593		90		
Unity-gain bandwidth					800		kHz
Common-mode rejection ratio	Error	V_{CC} = 40V, T_A = 25°C		65	80		dB
	Current-limit		CS-593		70		
Output sink current (pin 3)		V_{ID} = -15mV to -5 V, V (pin 3) = 0.5V		0.3	0.7		mA
Output source current (pin 3)		V_{ID} = 15mV to 5 V, V (pin 3) = 3.5 V		-2			mA

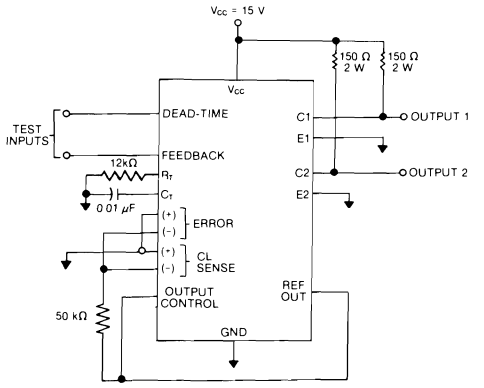
†Duration of the short-circuit should not exceed one second.

PARAMETER		TEST CONDITIONS	CS-593 C; CS-594 C; CS-595 C			UNIT
			MIN	TYP	MAX	
Output Section						
Collector off-state current		V_{CE} = 40V, V_{CC} = 40V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40V, V_E = 0			-100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15V, I_E = -200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5	mA
Output current voltage-lockout condition		V_{CC} = 1 V to 3 V, V (pin 4) = 0V V_C = 15V, V_E = 0V, V (output control) = 0V		4	200	μA

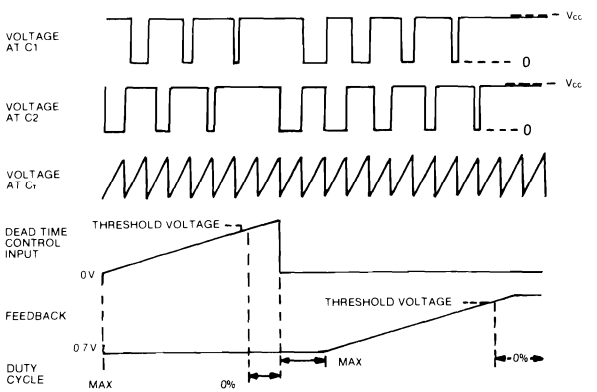
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
PWM Comparator section (see figure 1)						
Input threshold voltage (pin 3)	Zero duty cycle			4	4 5	V
Input sink current (pin 3)	V (pin 3) = 0.5V		0 3	0 7		mA
Under-Voltage Lockout						
Value @ T_A = 25°C					6	V
Value @ Full Temp			3 5		6.9	V
Hysteresis			100			mV
Steering Control (CS-595 only)						
Input current Pin 13	V_I = 0.4 V				-200	μA
	V_I = 2.4 V				200	
Zener-Diode Circuit (CS-595 only)						
Breakdown voltage	V_{CC} = 41V, I_Z = 2 mA			39		V
Sink current	V_I (pin 15) = 1 V			0 3		mA
Total Device						
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	V (pin 4) = 2 V, See Figure 1			12 4		mA
Switching Characteristics, T_A = 25° C						
Output voltage rise time	Common-emitter configuration, See Figure 3			100	200	ns
Output voltage fall time				30	100	ns
Output voltage rise time	Emitter-follower configuration, See figure 4			200	400	ns
Output voltage fall time				45	100	ns

PARAMETER MEASUREMENT INFORMATION

FIGURE 1—DEAD-TIME AND FEEDBACK CONTROL



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2—AMPLIFIER CHARACTERISTICS TEST CIRCUIT

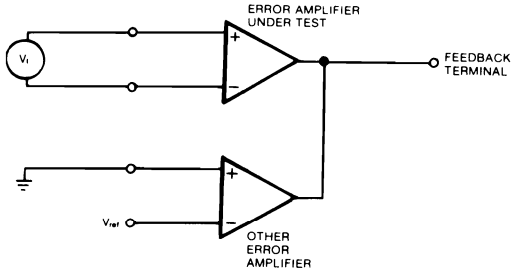
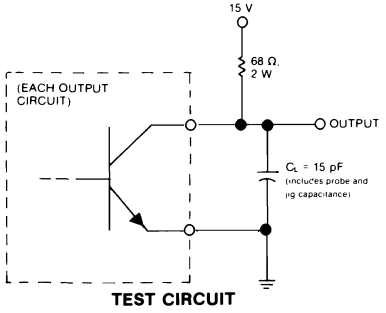
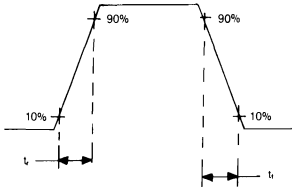


FIGURE 3—COMMON-EMITTER CONFIGURATION

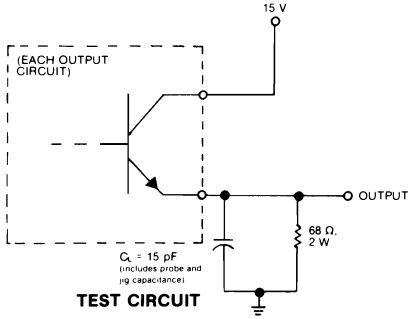


TEST CIRCUIT

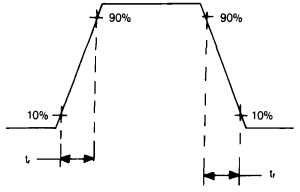


OUTPUT VOLTAGE WAVEFORM

FIGURE 4—EMITTER-FOLLOWER CONFIGURATION



TEST CIRCUIT



OUTPUT VOLTAGE WAVEFORM

4

TYPICAL CHARACTERISTICS

FIGURE 5

OSCILLATOR FREQUENCY VERSUS TIMING RESISTANCE

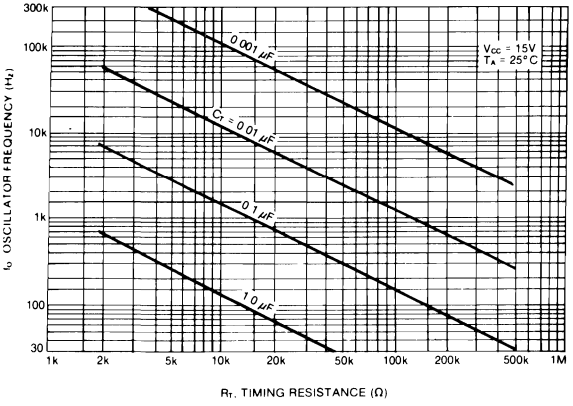
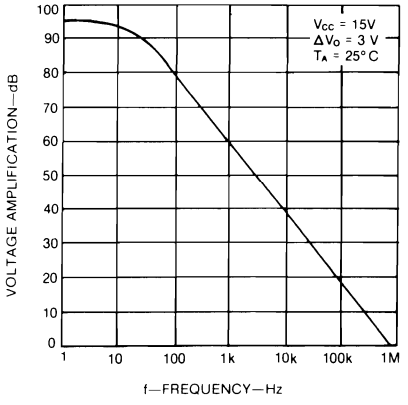


FIGURE 6

AMPLIFIER VOLTAGE AMPLIFICATION VERSUS FREQUENCY



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-593CJ	16 Lead CDIP
CS-593CN	16 Lead PDIP
CS-594CJ	16 Lead CDIP
CS-594CN	16 Lead PDIP
CS-595CJ	18 Lead CDIP
CS-595CN	18 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-3524

PULSE WIDTH MODULATOR CONTROL CIRCUIT

DUAL OUTPUT FOR SINGLE-ENDED OR PUSH-PULL APPLICATIONS

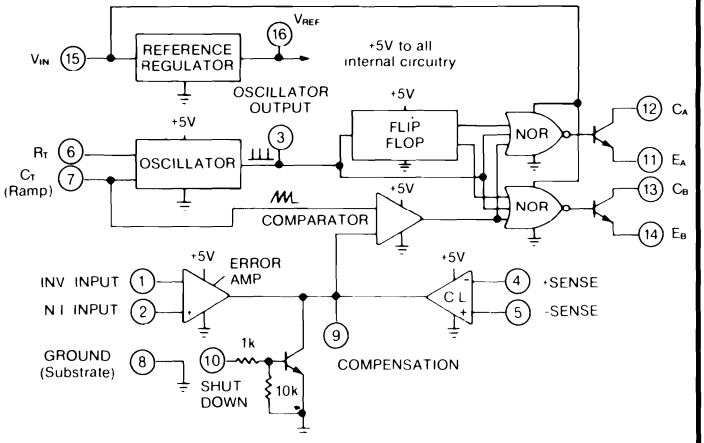
DESCRIPTION

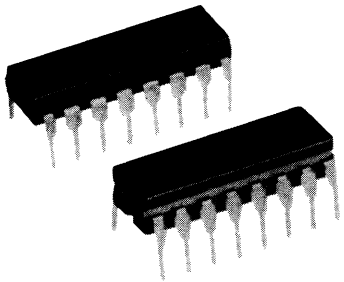
The CS-3524 incorporates all the functions required for the control of regulating power supplies, inverters or switching regulators. It can also be used as the control element for high-power-output applications. The CS-3524 is designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The CS-3524 is designed for operation from 0°C to + 70°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}	8V to 40V
Reference Output Current	0 to 20mA
Current through C_T Terminal	-0.03mA to -2mA
Timing Resistor, R_T	1.8KΩ to 100KΩ
Timing Capacitor, C_T	0.001μF to 0.1μF

BLOCK DIAGRAM

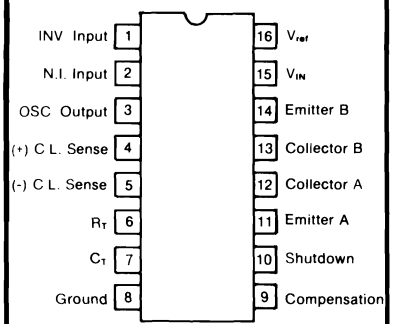




FEATURES:

- Complete PWM Control Circuit
- Single Ended or Push-Pull Outputs
- Low Standby Current (8mA Typical)
- 5V ± 4% Reference
- 1% Temperature Stability, V_{ref}
- Operation to 300 KH_Z
- Current Limiting

PIN CONNECTIONS



(Top View)

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 40V
Collector Output Current 100mA
Reference Output Current 50mA
Current Through C_T Terminal ..... -5mA

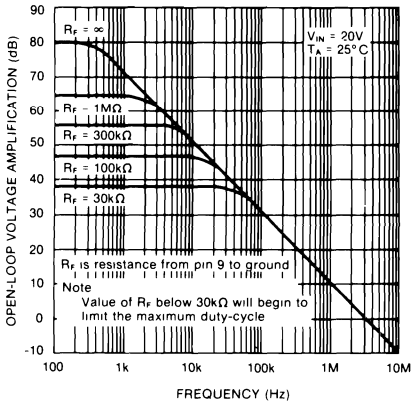
Power Dissipation at T_A = +25°C 1000mW
Derate Above 25°C ..... 8mW/°C
Storage Temperature Range ..... -65 to +150°C
Operating Junction Temperature ..... -55 to +150°C

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for 0°C to +70°C, V_{IN} = 20V, and f = 20kHz)

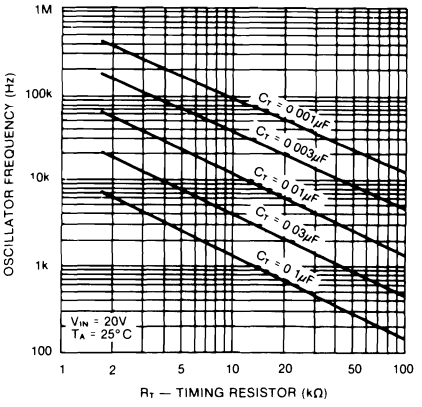
PARAMETER	TEST CONDITIONS	CS-3524			UNIT
		MIN.	TYP.	MAX.	
Reference Section					
Output Voltage		4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40V		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50	mV
Ripple Rejection	f = 120Hz, T_A = 25°C		66		dB
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C		100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1	%
Long Term Stability	T_A = 25°C, t = 1000 Hrs.		20		mV
Oscillator Section					
Maximum Frequency	C_T = .001μF, R_T = 2kΩ		300		kHz
Initial Accuracy	R_T and C_T Constant		5		%
Voltage Stability	V_{IN} = 8 to 40V, T_A = 25°C			1	%
Temperature Stability	Over Operating Temperature Range			2	%
Output Amplitude	Pin 3, T_A = 25°C		3.5		V
Output Pulse Width	C_T = .01μF, T_A = 25°C		0.5		μs
Error Amplifier Section					
Input Offset Voltage	V_{CM} = 2.5V		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10	μA
Open Loop Voltage Gain		60	80		dB
Common Mode Voltage	T_A = 25°C	1.8		3.4	V
Common Mode Rejection Ratio	T_A = 25°C		70		dB
Small Signal Bandwidth	A_V = 0dB, T_A = 25°C		3		MHz
Output Voltage	T_A = 25°C	0.5		3.8	V
Comparator Section					
Duty-Cycle	% Each Output On	0		45	%
Input Threshold	Zero Duty-Cycle		1		V
Input Threshold	Maximum Duty-Cycle		3.5		V
Input Bias Current			1		μA
Current Limiting Section					
Sense	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T_A = 25°C	180	200	220	mV
Sense Voltage T.C.			0.2		mV/°C
Common Mode Voltage		-1		+1	V
Reference Section					
Collector-Emitter Voltage		40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50	μA
Saturation Voltage	I_C = 50mA		1	2	V
Emitter Ouptut Voltage	V_{IN} = 20V	17	18		V
Rise Time	R_C = 2K ohm, T_A = 25°C		0.2		μs
Fall Time	R_C = 2K ohm, T_A = 25°C		0.1		μs
Total Standby Current (Excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10	mA

TYPICAL CHARACTERISTICS

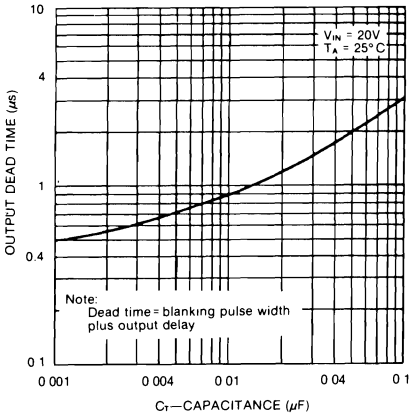
Open-Loop Voltage Amplification of Error Amplifier vs Frequency



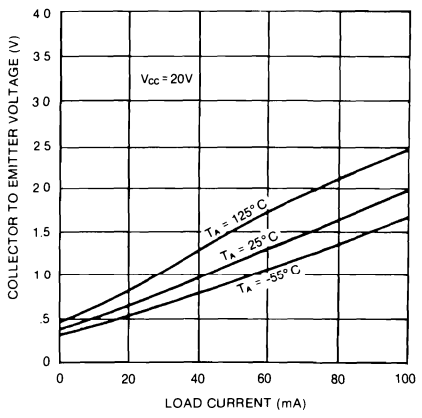
Oscillator Frequency vs Timing Components



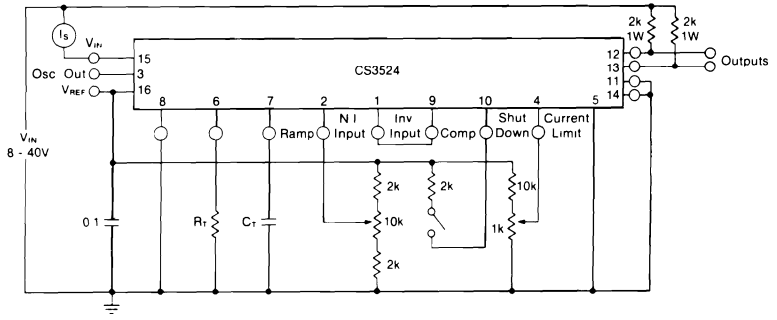
Output Dead Time vs Timing Capacitance Value



Output Saturation Voltage vs Load Current



OPEN LOOP TEST CIRCUIT



PRINCIPLES OF OPERATION

The CS3524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The CS3524 contains an on-board 5V regulator that serves as a reference as well as powering the CS3524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T.

The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to the oscillator . The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the CS3524 and is programmed by R_T and C_T according to the approximate formula:

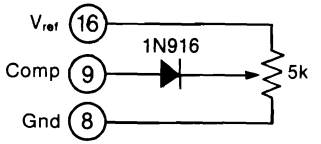
$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in kilhoms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:



Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more CS3524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Current Limiting

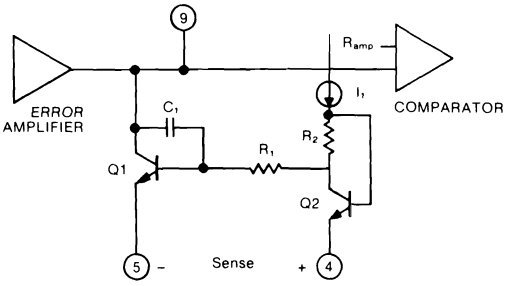
The current limiting circuitry of the CS3524 is shown below. By matching the base-emitter voltages of Q1 and Q2 and assuming negligible voltage drop across R_1.

$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2) = I_1R_2$$
$$\approx 200\ \text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line., Another factor to consider is that the frequency compensation provided by R_1 C_1 and Q1 provides a roll-off pole at approximately 300 Hertz.

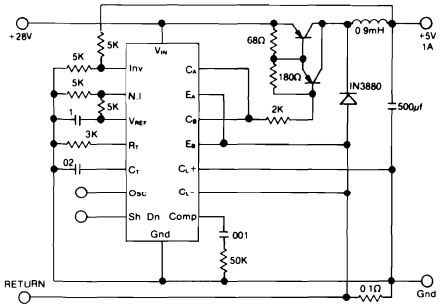
Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle witht the error amplifier signaling maximum duty cycle.

If this current limit circuitry is unused, pins 4 and 5 should both be grounded.



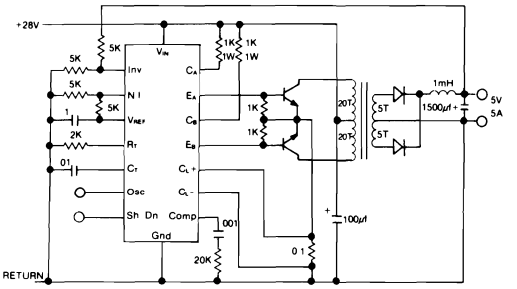
Current Limiting Circuitry of the CS3524

SINGLE-ENDED LC CIRCUIT



In this conventional single-ended regulator circuit, the two outputs of the CS3524 are connected in parallel for effective 0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.

PUSH-PULL TRANSFORMER COUPLED CIRCUIT



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the CS3524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

4

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-3524J	16 Lead CDIP
CS-3524N	16 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-3524A

PULSE WIDTH MODULATOR CONTROL CIRCUIT

ADVANCED VERSION OF INDUSTRY STANDARD

DESCRIPTION

The CS-3524A PWM control circuit retains the same versatile architecture of the industry standard CS-3524 (SG3524) while incorporating substantial improvements to many of its limitations.

The CS-3524 is pin-compatible with "non-A" versions, and in most applications can be directly interchanged. The CS-3524A, however, eliminates many of the design restrictions which had previously required additional circuitry.

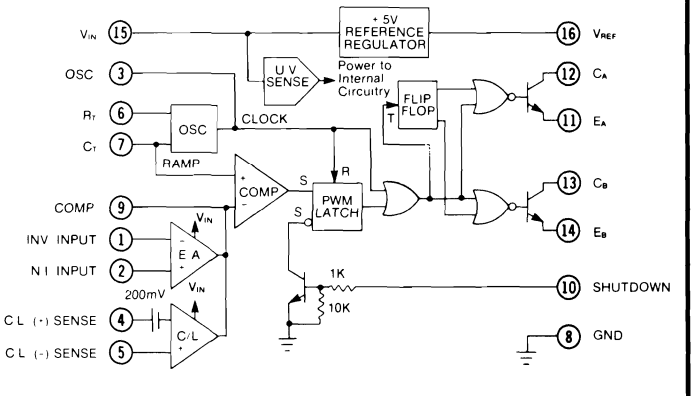
The CS-3524A includes a precision 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments, an error amplifier with an output voltage swing extending to 5V, and a current sense amplifier useful in either the ground or power supply output lines. The uncommitted 60V, 200mA NPN output pair greatly enhance the output drive capability.

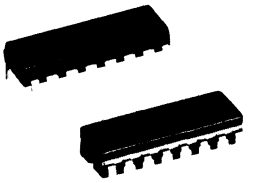
The CS-3524A features an under-voltage lockout circuit which disables all internal circuitry (except the reference) until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600 mV of hysteresis for jitter free activation.

Other improvements include a PWM latch that insures freedom from multiple pulsing within a period, even in noisy environments; logic to eliminate double pulsing on a single output, a 200 ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit is usable to 500 KHz and is now easier to synchronize with an external clock pulse.

The CS-3524A is rated for operation from 0 to 70° C, and is available in either ceramic or plastic packages.

BLOCK DIAGRAM

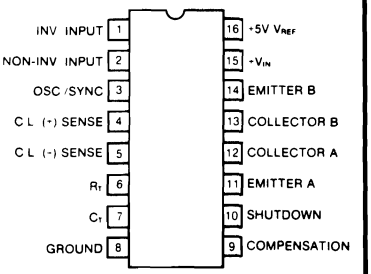




FEATURES:

- Fully interchangeable with standard CS-3524 family
- Precision reference internally trimmed to ±1%
- High-performance current limit function
- Under voltage lockout
- Start-up supply current less than 4mA
- Output current to 200mA
- 60V output capability
- Wide common-mode input range for both error and current limit amplifiers
- PWM latch insures single pulse per period
- Double pulse suppression logic
- 200ns shutdown through PWM latch
- Guaranteed frequency accuracy
- Thermal shutdown protection

PIN CONNECTIONS



(TOP VIEW)

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 60V
Output Current (Each Output) 200mA
Reference Output Current 50mA
Oscillator Charging Current 5mA

Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_C=+25°C 2000mW
Derate for Case Temperature above +25°C ..... 16mW/°C
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for 0°C to +70°C for the CS3524A; V_{IN} = V_C = 20V.)

PARAMETER	TEST CONDITIONS	CS-3524A			UNITS
		MIN.	TYP.	MAX.	
Turn-on Characteristics					
Input Voltage	Operating range after Turn-on	8		40	V
Turn-on Threshold		5.5	7.5	8.5	V
Turn-on Current	V_{IN} Turn-on - 100mV		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10	mA
Turn-on Hysteresis*			0.6		V
Reference Section					
Output Voltage	T_A = 25°C	4.90	5.00	5.10	V
Line regulation	V_{IN} = 10 to 40V		10	30	mV
Load Regulation	1_L = 0 to 20 mA		20	50	mA
Temperature Stability*	Over Operating Range		20	50	mV
Short Circuit Current	V_{REF} = 0, T_A = 25°C		80	100	mA
Output Noise Voltage*	10hz≤f≤10kHz, T_A = 25°C		40		μVrms
Long Term Stability*	T_A = 125°C = 1000 Hrs.		20	50	mV
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)					
Initial Accuracy	T_A = 25°C	39	43	47	kHz
Temperature Stability*	Over Operating Temperature Range		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			kHz
Output Amplitude*	T_A = 25°C		3.5		V
Output Pulse Width*	T_A = 25°C		0.5		μs
Ramp Peak		3.3	3.5	3.7	V
Ramp Valley		0.7	0.9	1.0	V
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)					
Input Offset Voltage			2	10	mV
Input Bias Current			1	10	μA
Input Offset Current			0.5	1	μA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	60	75		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	V
Open Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10 Meg Ω	60	80		dB
Gain-Bandwidth*	T_A = 25°C, A_V = 0dB		3		MHZ

*These parameters are guaranteed by design but not 100% tested in production.

ELECTRICAL CHARACTERISTICS (Continued)

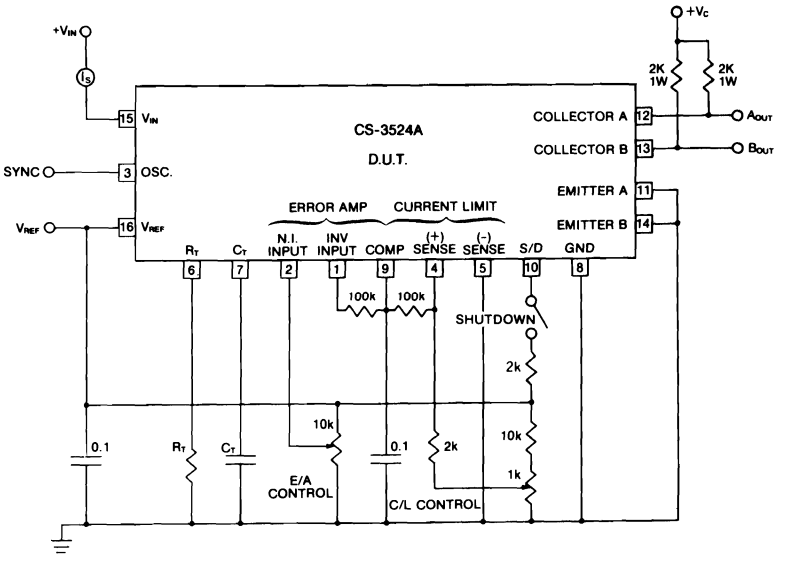
PARAMETER	TEST CONDITIONS	CS-3524A			UNITS
		MIN.	TYP.	MAX.	
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)					
Input Offset Voltage	T_A = 25°C, E/A Set for Max. Output	180	200	220	mV
Input Offset Voltage	Over Operating Temperature Range	170		230	mV
Input Bias Current			-1	-10	μA
Common Mode Rejection Ratio	$V_{(PIN\ 5)}$ = 0 to 15V	50	60		dB
Power Supply Rejection Ratio	$V_{(IN)}$ = 10 to 40V	50	60		dB
Output Swing	Minimum Total Range	0.5		5.0	V
Open Loop Voltage Gain	$\Delta V_{(O)}$ = 1 to 4V, $R_L \geq$ 10 Meg Ω	70	80		dB
Delay Time*	Pin 4 to Pin 9, $\Delta V_{(IN)}$ = 300mV		300		ns
Output Section (Each Output)					
Collector Emitter Voltage	I_C = 100μA	60	80		V
Collector Leakage Current	V_{CE} = 50V		1	20	μA
Saturation	I_C = 20mA I_C = 200mA		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		V
Rise Time*	T_A = 25°C, R = 2KΩ		200		ns
Fall Time*	T_A = 25°C, R = 2KΩ		100		ns
Comparator Delay*	T_A = 25°C, Pin 9 to Output		300		ns
Shutdown Delay*	T_A = 25°C, Pin 10 to Output		200		ns
Shutdown Threshold	T_A = 25°C, R_C = 2KΩ	0.5	.7	1.0	V
Thermal Shutdown*			165		°C

*These parameters are guaranteed by design but not 100% tested in production.

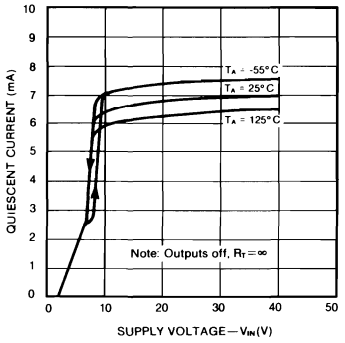
OPEN LOOP TEST CIRCUIT

Note: The CS3524A should be able to be tested in any 3524 test circuit with two possible exceptions:

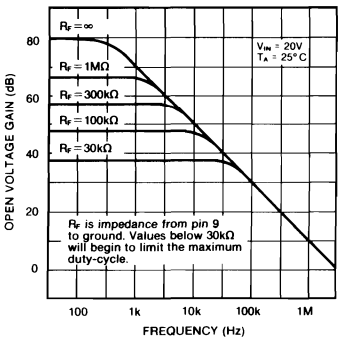
1. The higher gain-bandwidth of the current limit amplifier in the CS3524A may cause oscillations in an uncompensated 3524 test circuit.
2. The effect of the shutdown, pin 10, cannot be seen at the compensation terminal, pin 9, but must be observed at the outputs. The circuit below will allow all CS3524A functions to be evaluated.



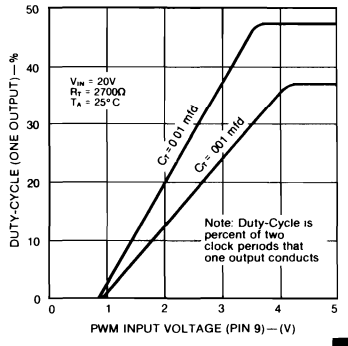
Supply Current vs Voltage



Error Amplifier Voltage Gain vs Frequency

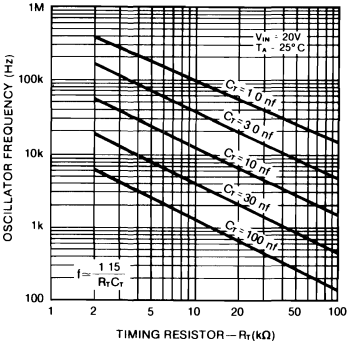


Pulse Width Modulator Transfer Function

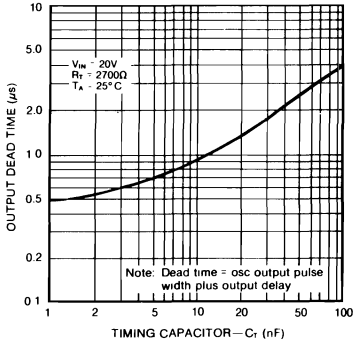


4

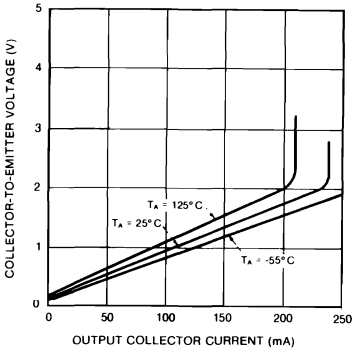
Oscillator Frequency vs Timing Components



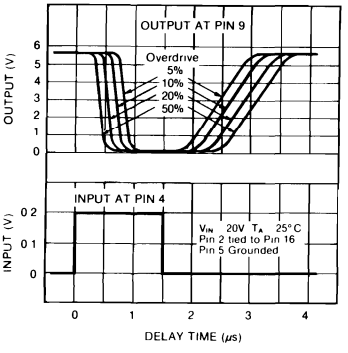
Output Dead Time vs Timing Capacitor Value



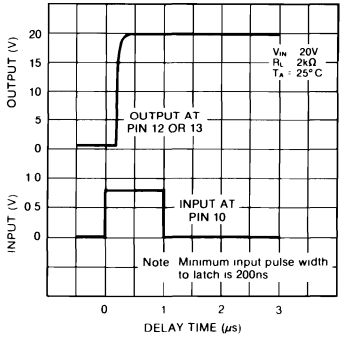
Output Saturation Voltage



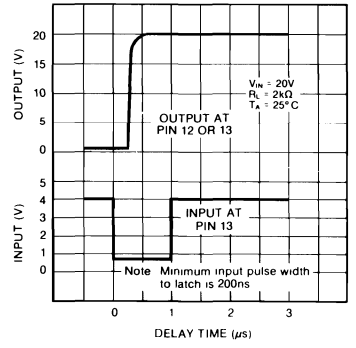
Current Limit Amplifier Delay



Turn-Off Delay From Shutdown—Pin 10



Shutdown Delay From PWM Comparator—Pin 9



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-3524AJ	16 Lead CDIP
CS-3524AN	16 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-320
CS-321

ONE MEGAHERTZ CURRENT-MODE CONTROL

DESCRIPTION

The CS-320/1 family of integrated circuits is designed for use with the most preferred types of current-mode control: Hysteretic, Constant-OFF Time, and Constant-Frequency. Careful consideration was given to each of the circuit blocks to allow operation at switching frequencies up to one megahertz.

Several protection features are included to ensure "bullet-proof" operation under severe operating conditions. When used in the Constant-OFF Time mode, a unique circuit (patent-pending) continually monitors the inductor current and extends the OFF time to prevent a current-runaway situation during overload conditions.

The precision timer circuit gives the power supply designer complete freedom in selecting the maximum ON/OFF time of the output drivers.

A programable UVLO is optimized for either OFF-line Boot-Strap or low voltage/battery operation.

The high-bandwidth voltage-type error amplifier has a novel bidirectional interface port that allows paralleling power modules without the need to assign "master/slave" status.

In the CS-320 the output is ACTIVE-HIGH, while the CS-321 is ACTIVE-LOW.

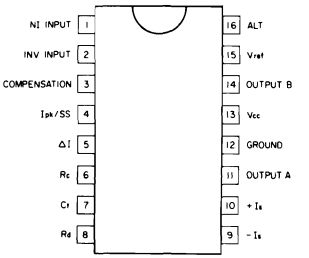
ABSOLUTE MAXIMUM RATINGS

Supply voltage 20V
Output current ..... ±1A
Analog Inputs ..... -0.25 to V_{CC} -4V

FEATURES:

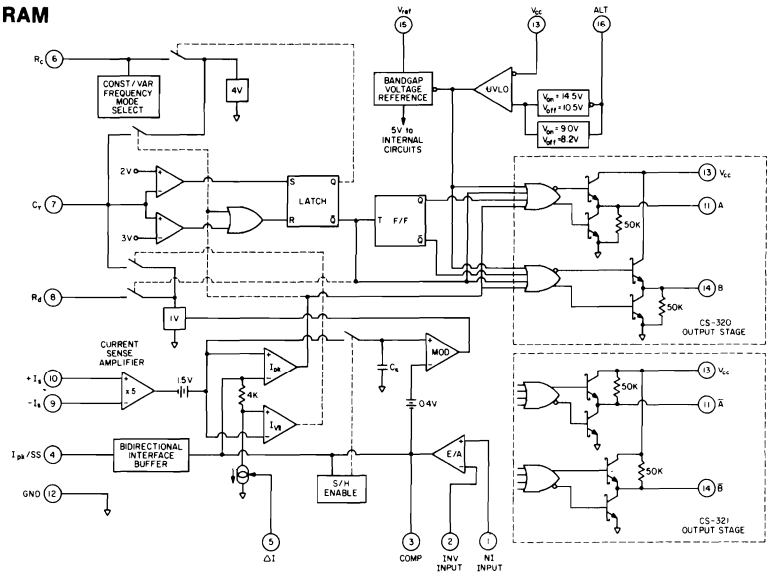
- One Megahertz Operation
- Programmable Under-Voltage Lockout
- Inherent protection against Current Runaway During Short Circuit Conditions
- Operates in Hysteretic, Constant-OFF time and Constant Frequency Modes
- Allows Parallel Operation of Power Modules without "Master/Slave" Status
- Optimized for interfacing with Current-Sensing MOSFETs

PIN CONNECTIONS



TOP VIEW

BLOCK DIAGRAM



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS Unless otherwise stated, specifications apply at -25≤Ta≤85°C for the CS320/1 I, 0≤Ta≤70°C for the CS320/1 C. V_{cc}=20V

PARAMETER	PIN	TEST CONDITIONS	CS-320/1 I			CS-320/1 C			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section									
Output Voltage	15	Tj=25 C Io=1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	15	V16=5V, 9.5<Vin<20V		5	20		5	20	mV
Load Regulation	15	1<Io<10mA		6	25		6	25	mV
Temp Stability	15	(Note 1)		0.2	0.6		0.2	0.6	mV/C
Total Output Variation	15	Line, Load, Temp	4.90		5.10	4.82		5.18	V
Output Noise Voltage	15	10Hz<f<10kHzTj=25C (Note 1)		50			50		uV
Long Term Stability	15	Ta=125 C, 1000 Hrs, (Note 1)		5	25		5	25	mV
Output Short Circuit	15	Ta=25 C V15=0V	25		120	25		125	mA
Timer Section Note: Rc=3.9k, Rd=4.7k, Ct=2000pF unless otherwise noted									
Maximum ON Time	7	Tj=25 C	4.50	5.00	5.50	4.50	5.00	5.50	uS
Maximum OFF Time	7	Tj=25 C	4.50	5.00	5.50	4.50	5.00	5.50	uS
Voltage Stability	7	V16=5V, 9.5<Vin<20V		1			1		%
Temp. Stability	7	Tmin<Ta<Tmax (Note 1)		5			5		%
Vpeak	7			2.9			2.9		V
Vvalley	7			2.0			2.0		V
Vcharge	6	I6=1mA, V7=1.5V		4.0			4.0		V
Vdischarge	8	I8=1mA, V7=3.5V		1.0			1.0		V
Maximum Charge Current	6	V6=2V, V7=1.5V	1.0			1.0			mA
Maximum Discharge Current	8	V8=3V, V7=3.5V	1.0			1.0			mA
Error Amp. Section									
Input Offset Voltage	1,2	V1=2.5V, V2=V3			10			15	mV
Input Bias Current	1,2	V1=V2=2.5V		-0.3	-1		-0.3	-2	uA
Input Offset Current	1,2	V1=V2=2.5V		0.1	1		0.1	1	uA
AVol	3	1<VO<3.5V	65	90		65	90		dB
Unity Gain Bandwidth	3	(Note 1)	3	6		3	6		MHz
Vout High	3		3.8	4		3.8	4		V
Vout Low	3			0.7	1.1		0.7	1.1	V
Common Mode Voltage Range	1,2		1.5		5.5	1.5		5.5	V
Current Sense Section									
Gain	9,10	V9=1V, V3=V2, (Note 2)	4.35	5.0	5.65	4.35	5.0	5.65	V/V
Max. Diff. Input Signal	9,10				400			400	mV
PSRR	9,10			70			70		dB
Input Bias Current	9,10			-40	-65		-40	-65	uA
Delay To Output	11,14	(Note 1)		100	150		100	150	nS
Com.-Mode Voltage Range	9,10		-0.25		Vcc-4	-0.25		Vcc-4	V
CMRR	9,10		60	80		60	80		dB
Current Hysteresis Input									
ΔI Current	5	V_s=OV		0.5	50		0.5	50	uA
Under-Voltage Lockout Section									
Start-Up Current	13			0.8	2		0.8	2	mA
Operating Supply Current	13			26	35		26	35	mA
Start Threshold (Hi)	13	V16=0V	13.5	14.5	15.5	13.5	14.5	15.5	V
Start Threshold (Lo)	13	V16=OPEN	8.5	9.0	9.5	8.5	9.0	9.5	V
Stop Threshold (Hi)	13	V16=0V	9.5	10.5	11.5	9.5	10.5	11.5	V
Stop Threshold (Lo)	13	V16=OPEN	7.4	8.2	8.8	7.4	8.2	8.8	V
Alt. Start Input Current	16	V16=0V	35	60	100	35	60	100	uA
Output Section (Note 3)									
Output Low Level	11,14	Isink=20mA		0.25	0.4		0.25	0.4	V
		Isink=200mA		1.5	2.2		1.5	2.2	V
Output High Level	11,14	Isink=20mA	18	18.5		18	18.5		V
		Isink=200mA	17.5	18		17.5	18		V
Rise Time	11,14	Tj=25 C C1=1nF (Note 1)		60	100		60	100	nS
Fall Time	11,14	Tj=25 C C1=1nF (Note 1)		30	60		30	60	nS
Output Resistance	11,14	Vin<Vin (Start)	35K	50K	65K	35K	50K	65K	Ohm
Ipeak/Soft-Start Section									
S/S Cap. Charge Current	4	V4=0V	40	75	115	40	75	115	uA

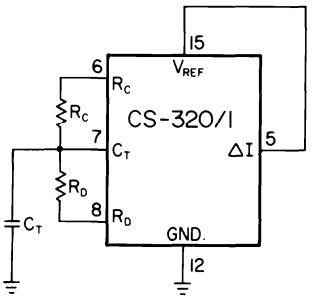
Note 1: Although guaranteed, these parameters are not 100% tested in production.

Note 2: Gain is defined as: $A = \frac{V3_2 - V3_1}{V10_2 - V10_1}$ Where: $V3_1$=2.5V, $V3_2$=3.5V

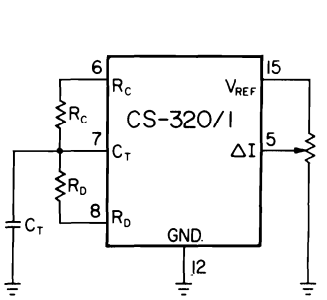
Measure $V10_1$ and $V10_2$ at turn OFF of output.

Note 3: CS-320 Output is active HIGH
CS-321 Output is active LOW

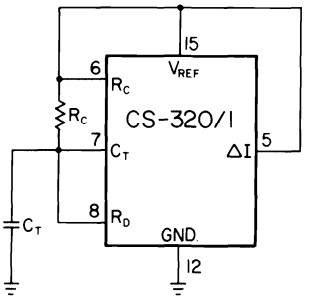
TYPICAL TIMER CONFIGURATIONS FOR THE THREE CURRENT-MODE CONTROLLERS



CONSTANT OFF TIME



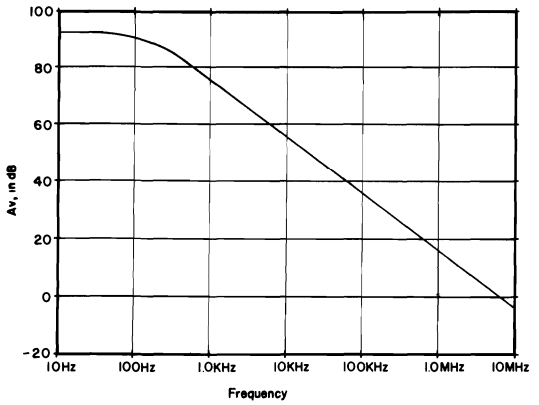
HYSTERETIC



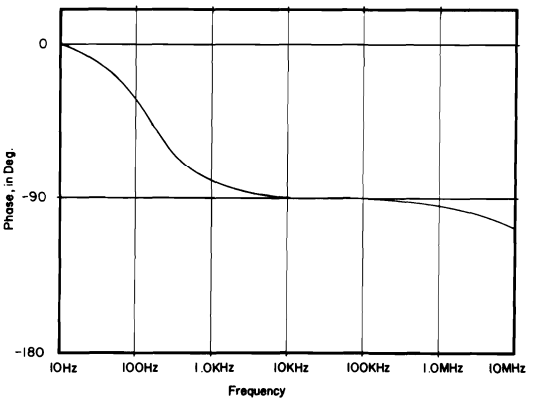
CONSTANT FREQUENCY

4

ERROR AMPLIFIER TYPICAL CHARACTERISTICS



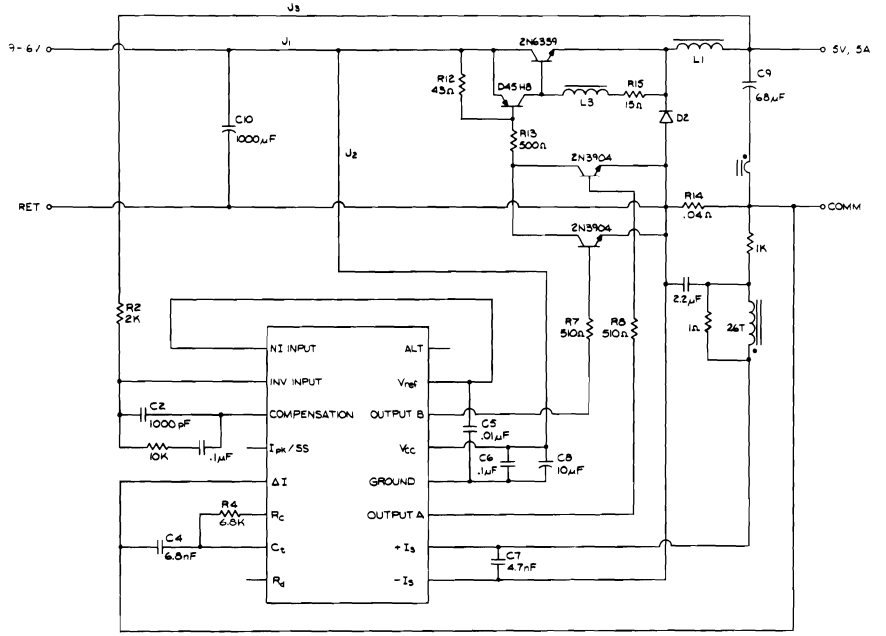
ERROR AMPLIFIER OPEN LOOP GAIN vs FREQUENCY



ERROR AMPLIFIER OPEN LOOP PHASE vs FREQUENCY

MANUFACTURED UNDER U.S. PATENT NO. 4,456,872

TYPICAL APPLICATION



STEP DOWN WITH HYSTERETIC CMC

ORDERING INFORMATION

PART NO.	0°C to 70°C	-25°C to 85°C	PACKAGE
CS-320CJ	*		16L CDIP
CS-320CN	*		16L PDIP
CS-321CJ	*		16L CDIP
CS-321CN	*		16L PDIP
CS-320IJ		*	16L CDIP
CS-320IN		*	16L PDIP
CS-321IJ		*	16L CDIP
CS-321IN		*	16L PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-322
CS-324

HYSTERETIC CURRENT-MODE CONTROLLER

DESCRIPTION

The CS-322/4 is designed for operating switching voltage regulators using hysteretic current-mode control. The difference between the CS-322 and the CS-324 is in the undervoltage lockout. The CS-322 is intended for off-line applications while the CS-324 is intended for battery input or DC to DC converters.

This IC allows the user to select the current hysteresis level required with a minimum of about 10% of full load. An uncommitted current sense amplifier (CSA) is available for performing accurate inductor current measurements. The error amplifier (E/A) has its non-inverting input committed to the ICs internal reference voltage. Trimming of the bandgap reference is done at the NI port of the E/A to achieve a ± 1% tolerance. The output stage provides sufficient current capability to interface directly with MOSFETs

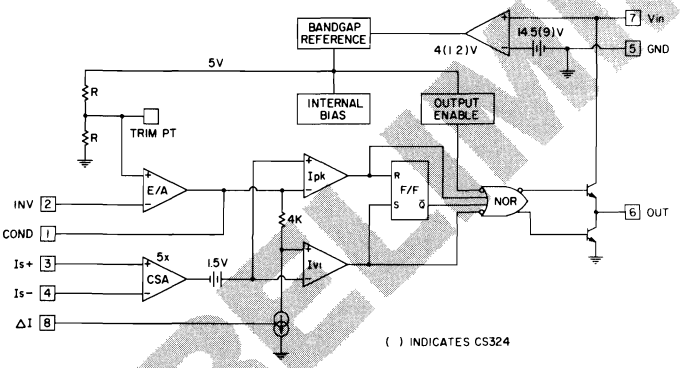
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20V
Output Current	±1A (peak)
	±200mA (steady state)

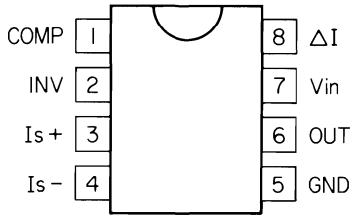
FEATURES:

- Provides hysteretic current-mode control.
- Inherent short circuit protection of power supply.
- High Current Totem Pole output.
- Eliminates right-half plane zero in continuous conduction flyback and boost converters.
- Allows feedforward of output current.

BLOCK DIAGRAM



PIN CONNECTIONS
8L PDIP/SO-8



ELECTRICAL CHARACTERISTICS Unless otherwise noted, specifications apply at -25≤Ta≤85°C for the CS322/4 I, 0≤Ta≤70°C for the CS322/4 C. V_{cc}=20V

PARAMETER	TEST CONDITIONS	CS-322/4 I			CS-322/4 C			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Undervoltage Lockout Section								
Start-Up Current			0.8	1.5		0.8	1.5	mA
Operating Supply Current			14	20		14	20	mA
Start Threshold								
CS-322		13.5	14.5	15.5	13.5	14.5	15.5	V
CS-324		8.5	9.0	9.5	8.5	9.0	9.5	V
Stop Threshold								
CS-322		9.5	10.5	11.5	9.5	10.5	11.5	V
CS-324		7.4	7.8	8.2	7.4	7.8	8.2	V
Error Amplifier Section								
Input Bias Current	V2 = 2.5V		-.3	-1		-.3	-1	uA
Avol	1< Vc < 3.5V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 1)	3	6		3	6		MHz
V_{out} HI		3.8	4		3.8	4		V
V_{out} LO			.7	1.1		.7	1.1	V
Reference Input Voltage	V1 = V2	2.47	2.50	2.53	2.45	2.50	2.55	V
Current Sense Amplifier								
Gain	V4 = 1V, V2 = V1	4.75	5.00	5.25	4.35	5.00	5.65	V/V
Maximum Input Signal		.45	0.5	.55	.45	0.5	.55	V
PSRR			70			70		dB
Input Bias Current			-40	-65		-40	-65	uA
Com-Mode Voltage Range		-.25		Vcc -5	-.25		Vcc -5	V
CMRR		60	80		60	80		dB
Hysteresis Level	(V8 = 0.25V, Note 3)	40	50	60	40	50	60	mV
Output Section								
Output Low Level	Isink = 20mA		.25	.4		.25	.4	V
	Isink = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	Isink = 20mA	18	18.5		18	18.5		V
	Isink = 200mA	17.5	18		17.5	18		V
Rise Time	T_j = 25C C = 1nF (Note 1)		30	60		30	70	ns
Fall Time	T_j = 25C C = 1nF (Note 1)		30	60		30	70	ns
Output Resistance	$V_{in} < V_{uvlo}$	35K	50K	65K	35K	50K	65K	Ohms

Note 1: Although guaranteed, these parameters are not 100% tested in production.

Note 2: Gain is defined as: A = [V1(2) - V1(1)] / [V3(2) - V3 (1)], where V1(2) = 3.5V and V1(1) = 2.5V.

Note 3: Input Hysteresis Level is defined as V3(2) - V3(1) at V(4) = 1V

ORDERING INFORMATION

PART NO.	0°C to 70°C	-25°C to 85°C	PACKAGE
CS-322CN	*		8L PDIP
CS-322CD	*		8L SO
CS-324CN	*		8L PDIP
CS-324CD	*		8L SO
CS-322IN		*	8L PDIP
CS-324IN		*	8L PDIP

MANUFACTURED UNDER U.S. PATENT NO. 4, 456, 872

CSC™ CHERRY SEMICONDUCTOR

CS-323
CS-325

CONSTANT OFF-TIME CURRENT-MODE CONTROLLER

DESCRIPTION

The CS-323/5 is designed for operating power supplies with constant Off-time current-mode control. The difference between the CS-323 and CS-325 is in the undervoltage lockout (uvlo). The CS-323 is intended for primary-side control of off-line converters whereas the CS-325 is intended to operate in battery input or DC to DC converters.

This IC has the capability to automatically protect the power switch from severe overload conditions in the power supply which cause the current to run away. A modulator similar to that of the CS-320 is included to monitor the current at pin 3 and extend the OFF time when the current exceeds about 110% of its full load value.

The output stage has sufficient drive current capability to interface directly with MOSFETS. The E/A has its NI input committed internally to an internal bandgap reference which is trimmed to 2.5V. (±1% tolerance)

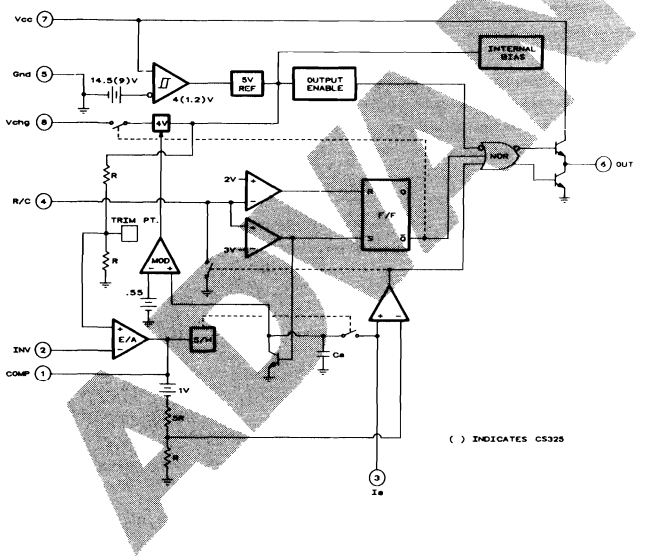
ABSOLUTE MAXIMUM RATINGS

Supply 20V
Output Current .....±1A (Peak)
.....±200mA (Steady State)

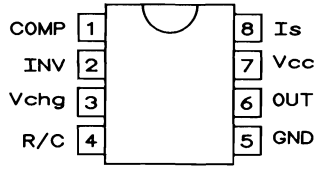
FEATURES:

- Provides Current-Mode Constant OFF time.
- Suitable for isolated and/or discontinuous conduction-mode converters.
- Eliminates right half plane zero in continuous conduction flyback and boost converters.

BLOCK DIAGRAM



PIN CONNECTIONS
8L PDIP/SO-8



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS Unless otherwise noted, specifications apply at -25≤Ta≤85°C for the CS323/5 I, 0≤Ta≤70°C for the CS323/5 C, V_{cc}=20V

PARAMETER	TEST CONDITIONS	CS-323/5 I			CS-323/5 C			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Undervoltage Lockout Section								
Start-Up Current			0.3	0.6		0.3	0.6	mA
Operating Supply Current			11	17		11	17	mA
Start Threshold								
CS-323		13.5	14.5	15.5	13.5	14.5	15.5	V
CS-325		8.5	9.0	9.5	8.5	9.0	9.5	V
Stop Threshold								
CS-323		9.5	10.5	11.5	9.5	10.5	11.5	V
CS-325		7.4	7.8	8.2	7.4	7.8	8.2	V
Error Amplifier Section								
Input Offset Voltage	V2 = V1			10			15	mV
Input Bias Current	V2 = 2.5V		-.3	-1		-.3	-1	uA
Input Offset Current	V2 = 2.5V		.1	1		.1	1	uA
Avol	1< Vc < 3.5V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 1)	3	6		3	6		MHz
V_{out} HI		3.8	4		3.8	4		V
V_{out} LO			.7	1.1		.7	1.1	V
Reference Input Voltage	V1 = V2	2.47	2.50	2.53	2.47	2.50	2.53	V
Current Sense Section								
Reflected Gain to E/A	V2 = V1 (Note 2)	5.7	6.0	6.3	5.7	6.0	6.3	V/V
Current Limit Clamp Threshold		.45	0.5	.55	.45	0.5	.55	V
PSRR			70			70		dB
Input Bias Current			-2	-10		-2	-10	uA
Delay to Output	(Note 1)		50	80		50	80	ns
Output Section								
Output Low Level	Isink = 20mA		.25	.4		.25	.4	V
	Isink = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	Isource = 20mA	18	18..5		18	18.5		V
	Isource = 200mA	17.5	18		17.5	18		V
Rise Time	T_j = 25C C1= 1nF		30	60		30	60	ns
Fall Time	T_j = 25C C1 = 1nF		30	60		30	60	ns
Output Resistance	$V_{in} < V_{uvlo}$	35	50	65	35	50	65	KOhms
Timer Section: Ct = 1nf, Rc = 4.3K, Rd = 16K								
Maximum OFF Time	T_j = 25C	4.5	5.0	5.5	4.5	5.0	5.5	us
Voltage Stability	9.5 < V_{in} < 20V		1			1		%
Temp. Stability	$T_{min} < T_a < T_{max}$ (Note 1)		5			5		%
V_{peak}			2.9			2.9		V
V_{valley}			2.0			2.0		V
V_{charge} (Pin 8)	I8 = 1mA, V4 = 1.5V		4.0			4.0		V
Maximum Charge Current, I8	V4 = 1.5V	1.0			1.0			mA

Note 1: Although guaranteed, these parameters are not 100% tested in production.

Note 2: Reflected Gain here is defined as: A = [V1(2) - V1(1)] / [V3(2) - V3 (1)], where V1(2) = 3.5V and V1(1) = 2.5V.

ORDERING INFORMATION

PART NUMBER	0°C to 70°C	-25°C to 85°C	PACKAGE
CS-323CN	*		8L PDIP
CS-323CD	*		8L SO
CS-325CN	*		8L PDIP
CS-325CD	*		8L SO
CS-323IN		*	8L PDIP
CS-325IN		*	8L PDIP

CSC™ CHERRY SEMICONDUCTOR

CS-1070

5A HIGH EFFICIENCY SWITCHING REGULATOR

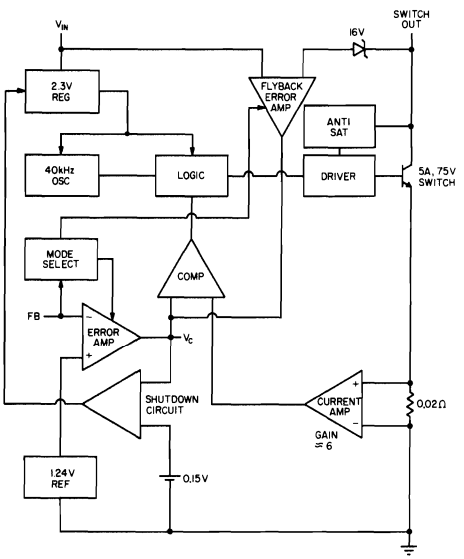
DESCRIPTION

The CS-1070 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the CS-1070 to be built in a standard TO-220 power package. This makes it extremely easy to use and provides "bust-proof" operation similar to that obtained with 3-pin linear regulators.

The CS-1070 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

The CS-1070 has many unique features not found even on the vastly more difficult to use low power control chips presently available. An externally activated shutdown mode reduces total supply current to 50μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the CS-1070 without the need for opto-couplers or extra transformer windings.

BLOCK DIAGRAM

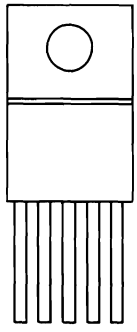


FEATURES:

- Wide Input Voltage Range 3V-60V
- Low Quiescent Current - 6mA
- Internal 5A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50μA Supply Current
- Flyback-Regulated Mode Has Fully Floating Outputs
- Comes in Standard TO-220 Package
- Can be Externally Synchronized

PIN CONNECTIONS

Tab (Gnd)



1 2 3 4 5

1 V_C
2 FB
3 Ground
4 V_{SW}
5 V_{IN}

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
(401) 885-3600 Telefax (401) 885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
CS-1070 ..... 60V
Switch Output Voltage
CS-1070 ..... 65V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Operating Temperature Range
CS-1070 ..... 0°C to +100°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.
• Denotes the specifications which apply from 0°C to +100°C.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		•	1.214	1.244	1.274	
Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
		•			1100	nA
Error Amplifier	ΔI_c = ±25μA		3000	4400	6000	μmho
Transconductance		•	2400		7000	μmho
Error Amplifier Source or	V_C = 1.5V		150	200	350	μA
Sink Current		•	120		400	μA
Error Amplifier Clamp	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
Voltage	Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.5	V
Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ 60V	•			0.03	%/V
Error Amplifier Voltage Gain	0.7V ≤ V_C ≤ 1.4V		500	800	2000	V/V
Minimum Input Voltage		•		2.6	3.0	V
Supply Current	3V ≤ V_{IN} ≤ 60V, V_C = 0.6V			6	9	mA
Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.05	V
		•	0.6		1.2	V
Normal/Flyback Threshold			0.4	0.45	0.52	V
on Feedback Pin						
Flyback Reference Voltage	I_{FB} = 50μA		15	16.3	17.6	V
		•	14		18	V
Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	8.5	V
Flyback Reference Voltage	I_{FB} = 50μA			0.01	0.03	%/V
Line Regulation	3V ≤ V_{IN} ≤ 60V					
Flyback Amplifier Transconductance	ΔI_C = ±10μA		150	300	500	μmho
Flyback Amplifier Source	V_C = 1.5V Source	•	15	32	50	μA
and Sink Current	I_{FB} = 50μA Sink	•	25	40	70	μA

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-1070	TO220

ELECTRICAL CHARACTERISTICS: (Continued) Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open. • Denotes the specifications which apply from 0°C to +100°C.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Switch Breakdown Voltage	$3V \leq V_{IN} \leq 60V$, I_{SW} = 5mA	•	65	90		V
Output Switch (Note 1) "On" Resistance	I_{SW} = 5A			0.15	0.24	Ω
Control Voltage to Switch Current Transconductance				8		A/V
Switch Current Limit	Duty Cycle = 50%	•	5		13	A
	50% < Duty Cycle = 80%	•	4		10	A
Supply Current Increase During Switch On-Time				25	35	mA/A
Switching Frequency			35	40	45	kHz
		•	33		47	kHz
Maximum Switch Duty cycle			90	92	97	%
Flyback Sense Delay Time				1.5		μs
Shutdown Mode Supply Current	$3V \leq V_{IN} \leq 60V$ V_C = 0.05V			100	250	μA
Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq 60V$		100	150	250	mV
		•	50		300	mV

Note 1: Measured with V_c in hi clamp, V_{FB} = 0.8V.

4

CS-1070 OPERATION

The CS-1070 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch curent reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the CS-1070. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the CS-1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The CS-1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the CS-1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regualtion.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the CS-1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50μA supply current for shutdown circuitry biasing.

CSC™ CHERRY SEMICONDUCTOR

CS-2841B

CURRENT MODE PWM CONTROL CIRCUIT

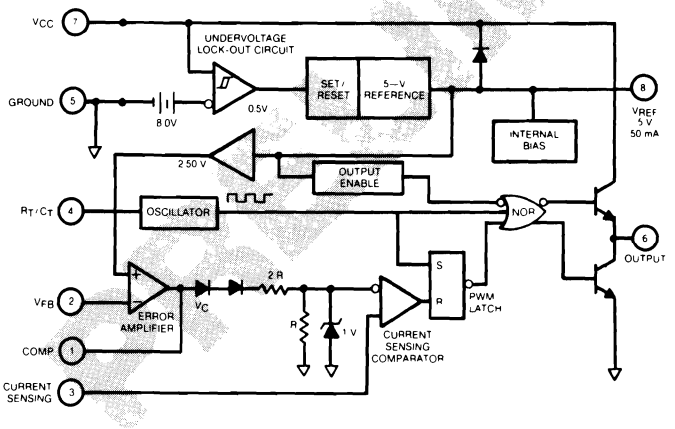
DESCRIPTION

The CS-2841B provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS-2841B is a variation of the CS-2843A designed specifically for use in automotive operation. The low start threshold voltage of typically 8.0V, and the ability to survive 42 volt automotive load dump transients are important for automotive subsystem designs. The CS-2841 series has a history of quality and reliability in automotive applications.

The CS-2841B incorporates a precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clamp eliminates any need for an external oscillator when at, or near, a 50% duty-cycle condition. Duty-cycles greater than 50% are also possible. Special logic ensures that Vref is stabilized before the output stage is enabled. Ion-implant resistors provide tighter control of under-voltage lockout.

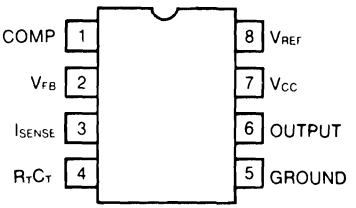
BLOCK DIAGRAM



FEATURES:

- Optimized for off-line control
- Internally trimmed temperature compensated oscillator
- Maximum duty-cycle clamp
- Vref stabilized before output stage is enabled
- Low start-up current
- Pulse-by-pulse current limiting
- Improved U/V lockout
- Double pulse suppression
- 1% trimmed bandgap reference
- High current totem pole output

PIN CONNECTIONS (TOP VIEW) DIP



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{cc}<30mA) ..... Self Limiting
Supply Voltage (Low Impedence Source) 30V
Output Current ..... ±1A
Output Energy (Capacitive Load) 5μJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3V to 5.5V
Error Amp Output Sink Current 10mA

ELECTRICAL SPECIFICATIONS: Unless otherwise stated, specifications apply for -40≤Ta≤85°C
R_T=680Ω, C_T=.022μF for triangular mode, R_T=10K, C_T=3.3nf for sawtooth mode (see Fig. 3)

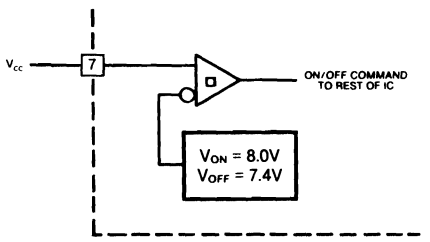
PARAMETER	TEST CONDITIONS	CS-2841B			UNITS
		MIN.	TYP.	MAX.	
Reference Section					
Output Voltage	T_j=25°C, I_o=1mA	4.90	5.00	5.10	V
Line Regulation	8.4≤V_{IN}≤16V		6	20	mV
Load Regulation	1≤I_o≤20mA		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.82		5.18	V
Output Noise Voltage	10Hz≤f≤10kHz, T_j=25°C (Note 2)		50		μV
Long Term Stability	T_A=125°C, 1000 Hrs. (Note 2)		5	25	mV
Output Short Circuit	T_A=25°C	-30	-100	-180	mA
Oscillator Section					
Initial Accuracy	Sawtooth Mode: (See Fig. 3)T_j=25°C	47	52	57	kHz
	Sawtooth Mode: -40°C≤T_a≤+85°	44	52	60	kHz
	Triangular Mode (see Fig. 3), T_j=25°C	44	52	60	kHz
Voltage Stability	8.4V≤V_{cc}≤16V		0.2	1	%
Temp. Stability	Sawtooth Mode T_{MIN}≤T_A≤T_{MAX} (Note 2)		5		%
	Triangular Mode T_{MIN}≤T_A≤T_{MAX} (Note 2)		8		%
Amplitude	V_{OSC}peak to peak		1.7		V
Discharge Current	T_j=25°C	7.4	8.3	9.2	mA
	T_{MIN}≤Ta≤T_{MAX}	7.2		9.4	mA
Error Amp Section					
Input Voltage	V_{COMP}=2.5V	2.42	2.50	2.58	V
Input Bias Current	V_{FB}= 0V		-0.3	-2	μA
A_{VOL}	2≤V_O≤4V	65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		MHz
PSRR	8.4≤V_{CC}≤16V	60	70		dB
Output Sink Current	V_{FB}=2.7V, V_{COMP}=1.1V	2	6		mA
Output Source Current	V_{FB}=2.3V, V_{COMP}=5V	-0.5	-0.8		mA
V_{OUT} High	V_{FB}=2.3V, R_L=15K to ground	5	6		V
V_{OUT} Low	V_{FB}=2.7V, R_L=15K to Pin 8		0.7	1.1	V
Current Sense Section					
Gain	(Notes 3 & 4)	2.85	3	3.15	V/V
Maximum Input Signal	V_{COMP}=5V (Note 3)	0.9	1	1.1	V
PSRR	8.4≤V_{CC}≤16V (Note 3)		70		dB
Input Bias Current	V_{SENSE}= 0V		-2	-10	μA
Delay to Output	T_j=25° (Note 2)		150	300	ns
Output Section					
Output Low Level	I_{SINK}=20mA		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2	V
Output High Level	I_{SOURCE}=20mA	13	13.5		V
	I_{SOURCE}=200mA	12	13.5		V
Rise Time	T_j=25°C, C_L=1nF (Note 2)		50	150	ns
Fall Time	T_j=25°C, C_L=1nF (Note 2)		50	150	ns
Output Leakage	V_{CC}=14V, UVLO Active, $V_{PIN\ 6}$=0		-0.01	-10	μA
Total Standby Current					
Start-Up Current			0.5	1	mA
Operating Supply Current	V_{FB}=V_{SENSE}=0V R_T=10K, C_T=3.3nF		11	17	mA

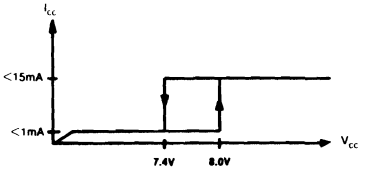
Notes: 1. Adjust V_{CC} above the start threshold before setting at 15V.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2}$=0.
4. Gain defined as:

$$A=\frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}};0\le V_{PIN\ 3}\le 0.8V.$$

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	CS-2841B			UNITS
		MIN.	TYP.	MAX.	
Under-Voltage Lockout Section					
Start Threshold		7.6		8.4	V
Min. Operating Voltage	AfterTurn On	7.0		7.8	V





During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. The output should be shunted to ground with a bleeder resistor to prevent output leakage current from activating the power switch.

Fig. 1

TIMING DIAGRAM

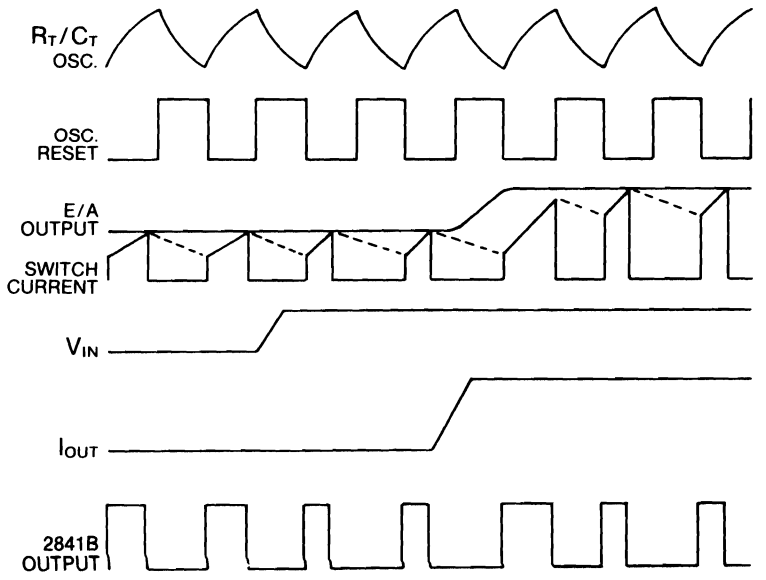


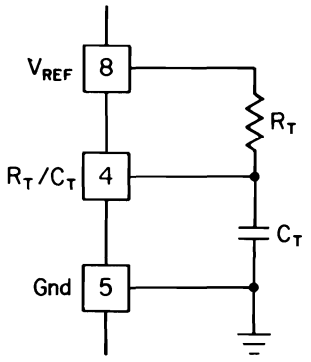
Fig. 2

NOTES ON CS-2841B TIMING DIAGRAM

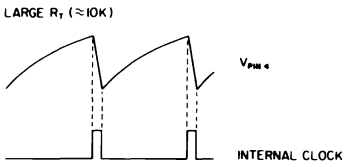
To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current. An increase in V_{IN} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of R_T/C_T components.

APPLICATIONS INFORMATION



Sawtooth Mode



Triangular Mode

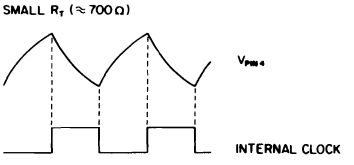
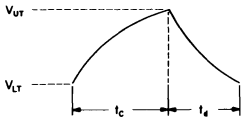


Fig. 3

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the LO state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:



$$t_c = R_T C_T \ell n \left(\frac{V_{REF} - V_{LT}}{V_{REF} - V_{UT}} \right)$$

$$t_d = R_T C_T \ell n \left(\frac{V_{REF} - I_d R_T - V_{UT}}{V_{REF} - I_d R_T - V_{LT}} \right)$$

Assuming typical values for the parameters in the above formulas:

V_{REF}=5.0V, V_{UT}=2.7V, V_{LT}=1.0V, I_d=8.3A, then

$$t_c \approx .5534\ R_T C_T$$

$$t_d \approx R_T C_T \ell n \left(\frac{2.3 - .0083 R_T}{4.0 - .0083 R_T} \right)$$

The frequency and maximum duty cycle can be approximately determined from the following graphs

OSCILLATOR FREQUENCY VS. C_T

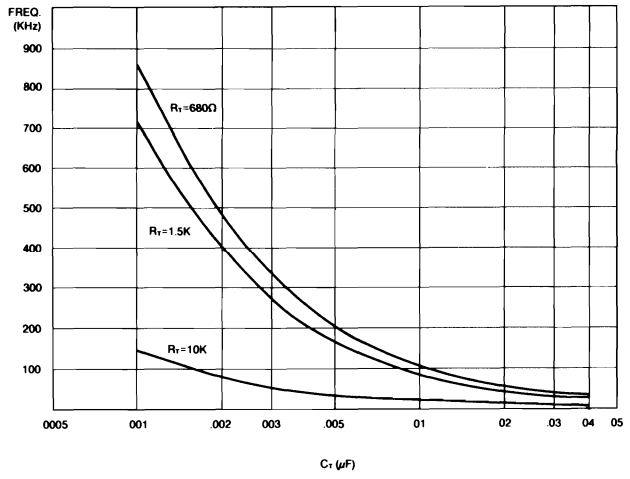


Fig. 4

OSCILLATOR DUTY CYLCLE VS. R_T

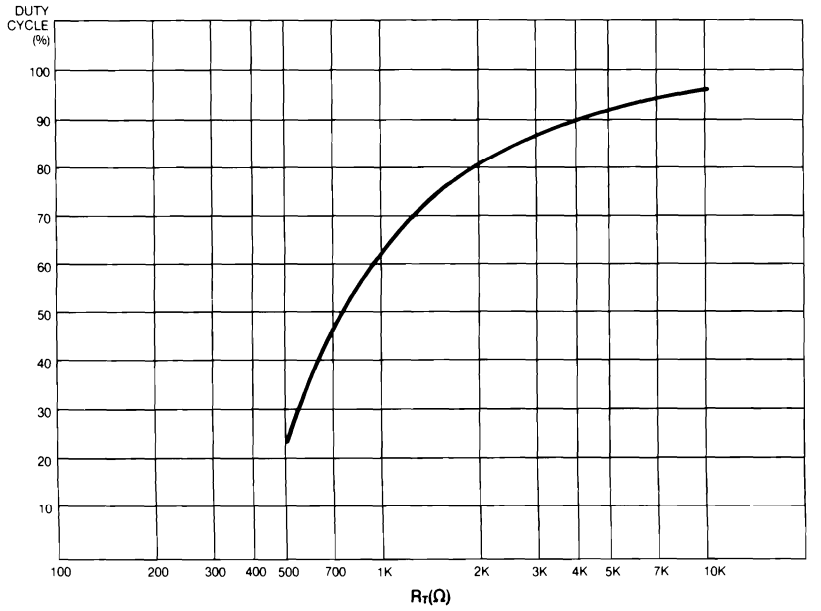
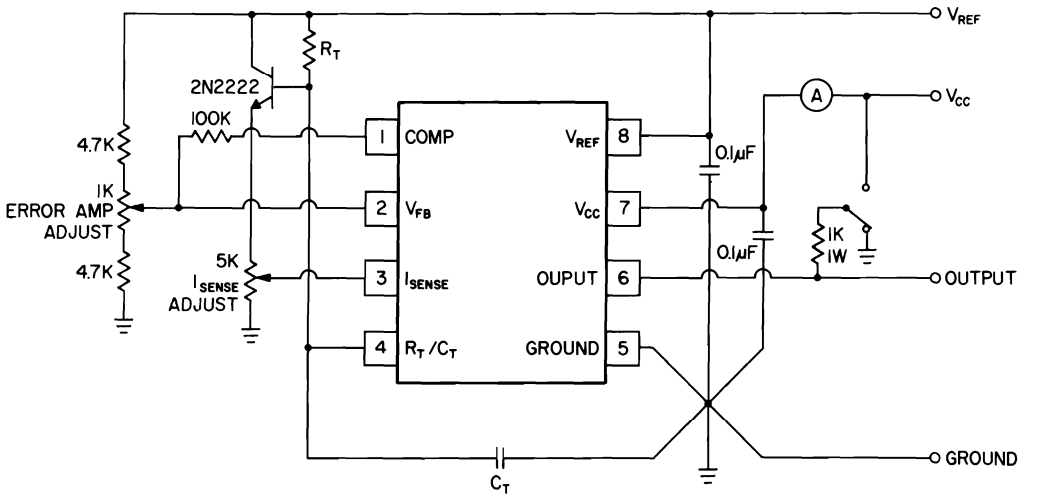


FIG. 5

OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

ORDERING INFORMATION

PART NUMBER	PACKAGE
CS-2841B	8L PDIP

CSC™ CHERRY SEMICONDUCTOR

CS-2842A/CS-3842A
CS-2843A/CS-3843A

CURRENT MODE PWM CONTROL CIRCUIT

DESCRIPTION

The CS-3842A provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS-3842A family incorporates a new precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clamp eliminates any need for an external oscillator when at, or near, a 50% duty-cycle condition. Duty-cycles greater than 50% are also possible. Special logic ensures that Vref is stabilized before the output stage is enabled. Ion-implant resistors provide tighter control of under-voltage lockout..

Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as the gate of power MOSFET. The output is low in the off state, consistent with N-channel devices.

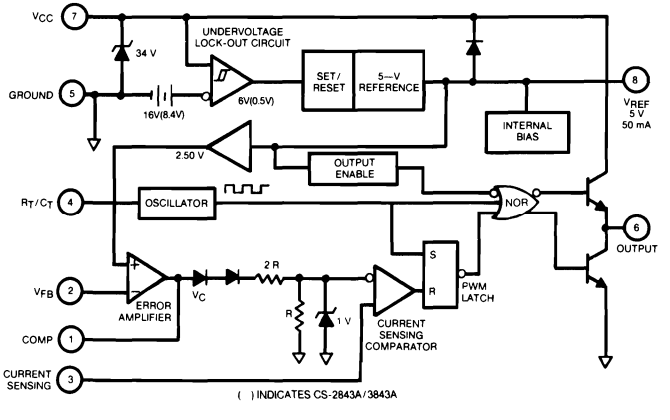
The CS-3842A series of current-mode control ICs are available in 14-pin and 16-pin "SO" package for surface mount applications as well as 8 pin PDIP and 8 pin CDIP.

ORDERING INFORMATION

PART NO.	0°C to 70°C	-25° to 85°C	PACKAGE
CS-3842AN	*		8LP DIP
CS-3842AD	*		14LSO
CS-3842ADW	*		16L SO WIDE
CS-2842AJ		*	8LC DIP
CS-2842AN		*	8LP DIP
CS-2842ADW		*	16L SO WIDE

PART NO.	0°C to 70°C	-25° to 85°C	PACKAGE
CS-3843AN	*		8LP DIP
CS-3843AD	*		14L SO
CS-3843ADW	*		16L SO WIDE
CS-2843AJ		*	8LC DIP
CS-2843AN		*	8LP DIP
CS-2843ADW		*	16L SO WIDE

BLOCK DIAGRAM

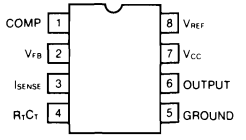


FEATURES:

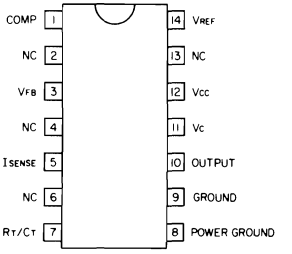
- Optimized for off-line control
- Internally trimmed temperature compensated oscillator
- Maximum duty-cycle clamp
- Vref stabilized before output stage is enabled
- Low start-up current
- Pulse-by-pulse current limiting
- Improved U/V lockout
- Double pulse suppression
- 1% trimmed bandgap reference
- High current totem pole output

PIN CONNECTIONS

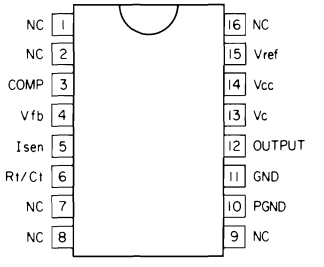
DIP/CDIP



SO-14



SO-16



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{cc}<30mA) ..... Self Limiting
Supply Voltage (Low Impedence Source) 30V
Output Current ..... ±1A
Output Energy (Capacitive Load) 5μJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3V to V_{cc}
Error Amp Output Sink Current 10mA

ELECTRICAL SPECIFICATIONS: Unless otherwise stated, specifications apply for -25≤Ta≤85°C for CS-2842A/2843A, 0≤Ta≤70°C for CS-3842A/3843A. Vcc=15V (Note 1); R_T=680Ω, C_T=.022μF for triangular mode, R_T=10K, C_T=3.3nf for sawtooth mode (see Fig. 3)

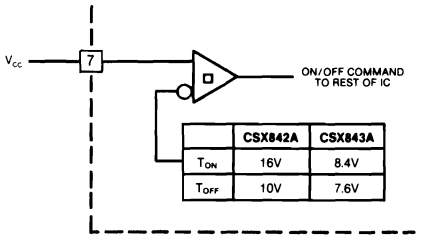
PARAMETER	TEST CONDITIONS	CS-2842A CS-2843A			CS-3842A CS-3843A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j=25°C, I_o=1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12≤V_{IN}≤25V		6	20		6	20	mV
Load Regulation	1≤I_o≤20mA		6	25		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	4.82		5.18	V
Output Noise Voltage	10Hz≤f≤10kHz, T_j=25°C (Note 2)		50			50		μV
Long Term Stability	T_A=125°C, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit	T_A=25°C	-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	Sawtooth Mode (see Fig. 3), T_j=25°C	47	52	57	47	52	57	kHz
	Triangular Mode (see Fig. 3), T_j=25°C	47	52	57	44	52	60	kHz
Voltage Stability	12≤V_{cc}≤25V		0.2	1		0.2	1	%
Temp. Stability	Sawtooth Mode T_{MIN}≤T_A≤T_{MAX} (Note 2)		5			5		%
	Triangular Mode T_{MIN}≤T_A≤T_{MAX} (Note 2)		8			8		%
Amplitude	$V_{PIN\ 4}$ peak to peak		1.7			1.7		V
Discharge Current	T_j=25°C	7.8	8.3	8.8	7.4	8.3	9.2	mA
	T_{MIN}≤Ta≤T_{MAX}	7.5		9.0	7.2		9.4	mA
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$=2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	2≤V_O≤4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
PSRR	12≤V_{CC}≤25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$=2.7V, $V_{PIN\ 1}$=1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$=2.3V, $V_{PIN\ 1}$=5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$=2.3V, R_L=15K to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$=2.7V, R_L=15K to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$=5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12≤V_{CC}≤25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output	T_j=25° (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=200mA	12	13.5		12	13.5		V
Rise Time	T_j=25°C, C_L=1nF (Note 2)		50	150		50	150	ns
Fall Time	T_j=25°C, C_L=1nF (Note 2)		50	150		50	150	ns
Output Leakage	V_{CC}=14V, UVLO Active, $V_{PIN\ 6}$=0		-0.01	-10		-0.01	-10	μA
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2}$=$V_{PIN\ 3}$=0V R_T=10K, C_T=3.3nF		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC}=25mA		34			34		V

Notes: 1. Adjust V_{CC} above the start threshold before setting at 15V.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2}$=0.
4. Gain defined as:

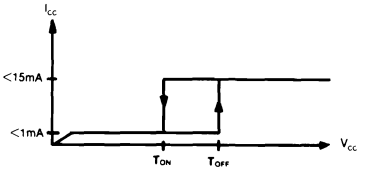
$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}} \quad ;0 \le V_{PIN\ 3} \le 0.8V.$$

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	CS-2842A			CS-3842A			CS-2843A CS-3843A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section											
Start Threshold		15	16	17	14.5	16	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9	10	11	8.5	10	11.5	7.0	7.6	8.2	V



	CSX842A	CSX843A
T_{ON}	16V	8.4V
T_{OFF}	10V	7.6V



During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent output leakage current from activating the power switch.

Fig. 1

3842A/3843A TIMING DIAGRAM

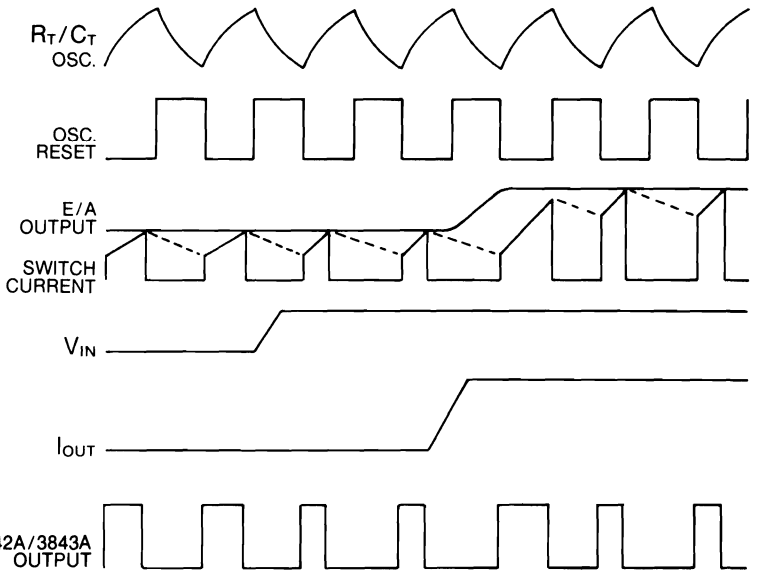


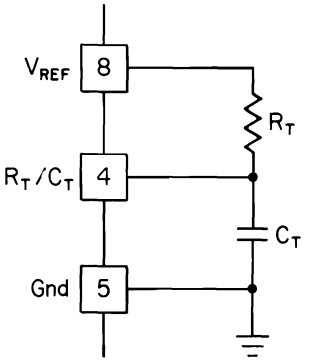
Fig. 2

NOTES ON CS3842A/CS3843A TIMING DIAGRAM

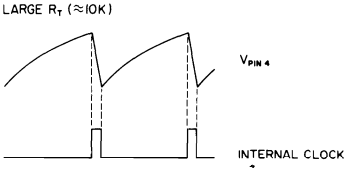
To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current. An increase in V_{IN} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of R_T/C_T components.

APPLICATIONS INFORMATION



Sawtooth Mode



Triangular Mode

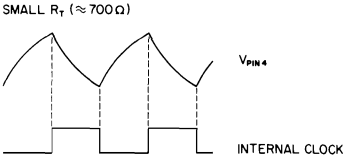
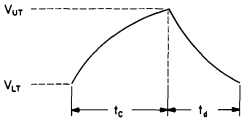


Fig. 3

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the LO state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:



$$t_c = R_T C_T \ell n \left(\frac{V_{REF} - V_{LT}}{V_{REF} - V_{UT}} \right)$$

$$t_d = R_T C_T \ell n \left(\frac{V_{REF} - I_d R_T - V_{UT}}{V_{REF} - I_d R_T - V_{LT}} \right)$$

Assuming typical values for the parameters in the above formulas:

V_{REF}=5.0V, V_{UT}=2.7V, V_{LT}=1.0V, I_d=8.3mA, then

$$t_c \approx .5534\ R_T C_T$$

$$t_d \approx R_T C_T \ell n \left(\frac{2.3 - .0083 R_T}{4.0 - .0083 R_T} \right)$$

The frequency and maximum duty cycle can be approximately determined from the following graphs

OSCILLATOR FREQUENCY VS. C_T

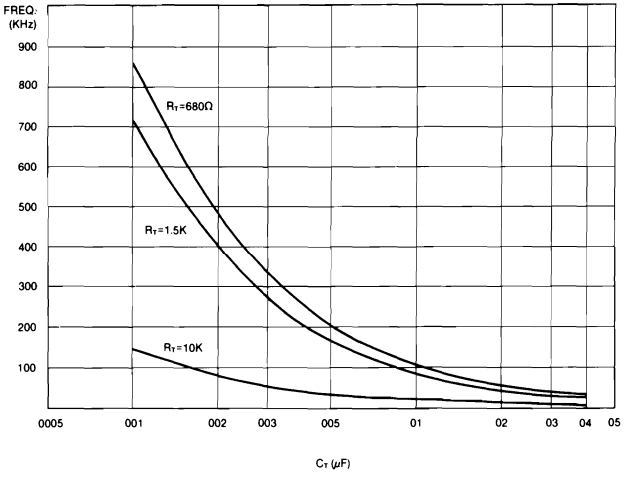


Fig. 4

OSCILLATOR DUTY CYLCLE VS. R_T

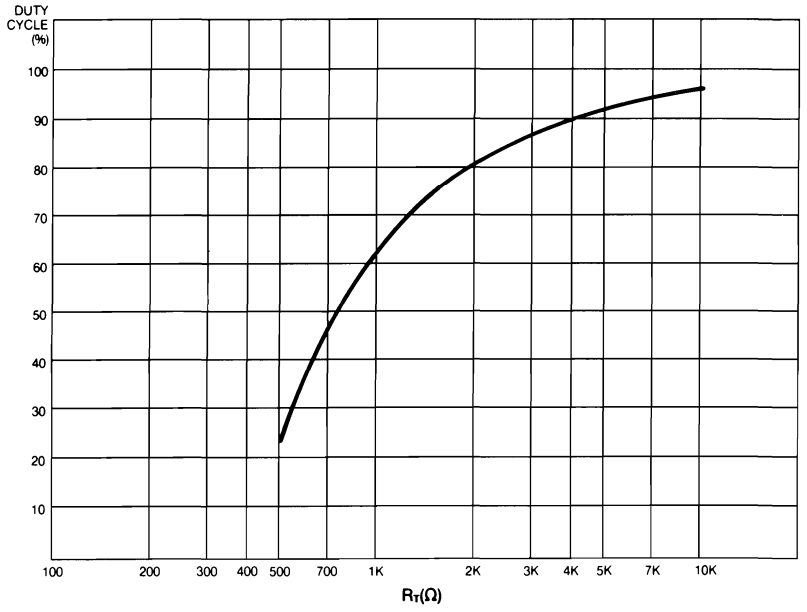
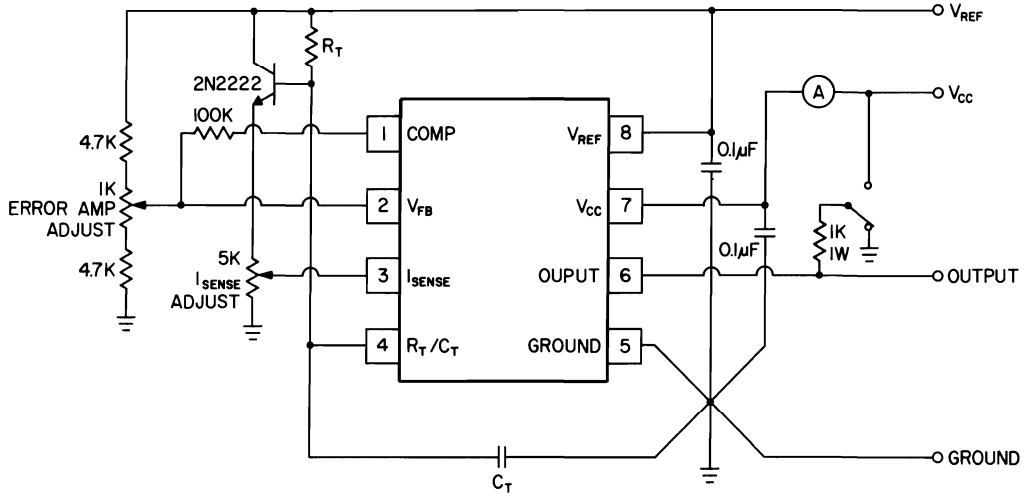


FIG. 5

OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

CHERRY SEMICONDUCTOR

APPLICATIONS NOTE

Single CS 3842A Provides Control For 500W 200 KHz Current Mode Power Supply

HERMAN NEUFELD

INTRODUCTION

With the introduction of Cherry's new CS-3842A PWM IC, current-mode is possible for power supplies of a wide range of output power levels. It's low cost makes the CS-3842A particularly attractive in low power DC to DC converter applications. But because this IC can provide a high output current (1A peak 200mA average) it is also capable of driving large power MOSFETS which in turn can switch high amounts of power

CURRENT-MODE VS. VOLTAGE-MODE CONTROL

In a switching power supply the output voltage is controlled by varying the conduction duty cycle of the power switch(es). Traditionally duty cycle control was done by comparing the amplified difference of the output voltage feedback signal and a fixed stable reference to a sawtooth waveform derived from an oscillator. This constitutes the basic voltage mode control scheme. It was later improved by allowing a sample of the input voltage to vary the slope of the sawtooth waveform. This feedforward scheme provides excellent line regulation in most of the popular circuit topologies. However, the task of compensating voltage mode converters has not been simple because of the resonant peak and 40dB/decade rolloff associated with the output LC filter.

In current mode control the control signal obtained from the error amplifier is compared with a signal representing the peak inductor current and forms a second loop in the circuit as shown in Figure 1. The advantages and disadvantages of current mode control are:

Advantages:

— Instantaneous correction to line voltage variations because the inductor current slope varies with input voltage.

— Since the peak inductor current is controlled the power supply behaves like a voltage controlled current source and the pole associated with the inductor is eliminated. This makes the power supply essentially stable to begin with.

— Equal current sharing in paralled power stages is possible when both share the same control signal and have the same current sense circuits.

— Due to the current limiting property of current-mode control a current limit amplifier is not necessary.

— Current-mode control provides flux balancing in push-pull circuits.

Disadvantages:

— Slope compensation is required for peak versus average inductor current error and to compensate for instabilities associated with load disturbances in single ended topologies operating at greater than 50% duty cycle.

The turn-ON current spike caused by the reverse diode recovery of the output free wheeling diode may cause premature shutdown. The circuit can also be susceptible to noise generated by the power switches.

— The half bridge topology is prone to a runaway condition when operated in current-mode control.

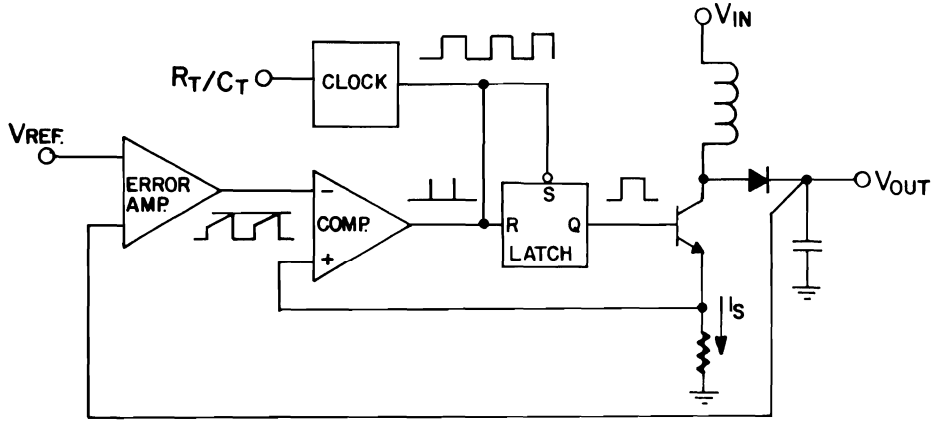
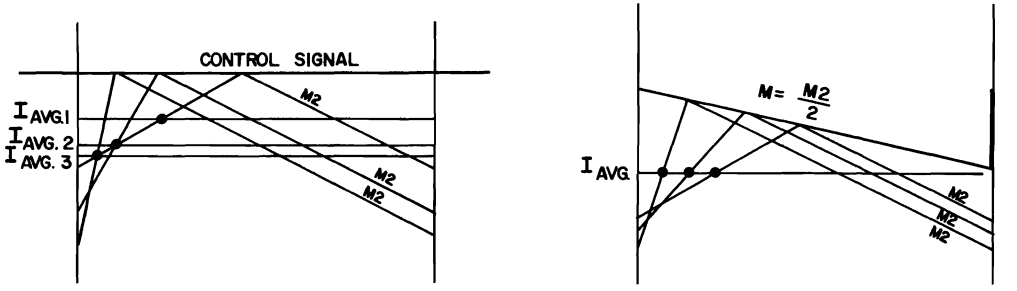


FIG.1 BASIC CIRCUIT ILLUSTRATING CURRENT - MODE CONTROL

If the current sense signal is properly filtered noise induced problems including the turn-ON spike can be avoided. By deliberately adding more slope to the current sense signal, or subtracting it from the control voltage signal, the instablity due to greater than 50% duty cycle operation can be overcome. Slope compensation also aids in reducing the uncertainty at the point of trigger in the PWM comparator when shallow current ramps are involved, and also helps the peak current appear higher than the turn-on spike thus eliminating premature shutdown. Figure 2A illustrates how the peak current detection scheme in current mode control produces a change in the average current when relying on the feedforward property of current mode to compensate for line voltage variations. If a slope equal to one-half the negative going inductor current slope is added to the current sense signal or subtracted from the control signal this error is corrected, as shown in Figure 2b.



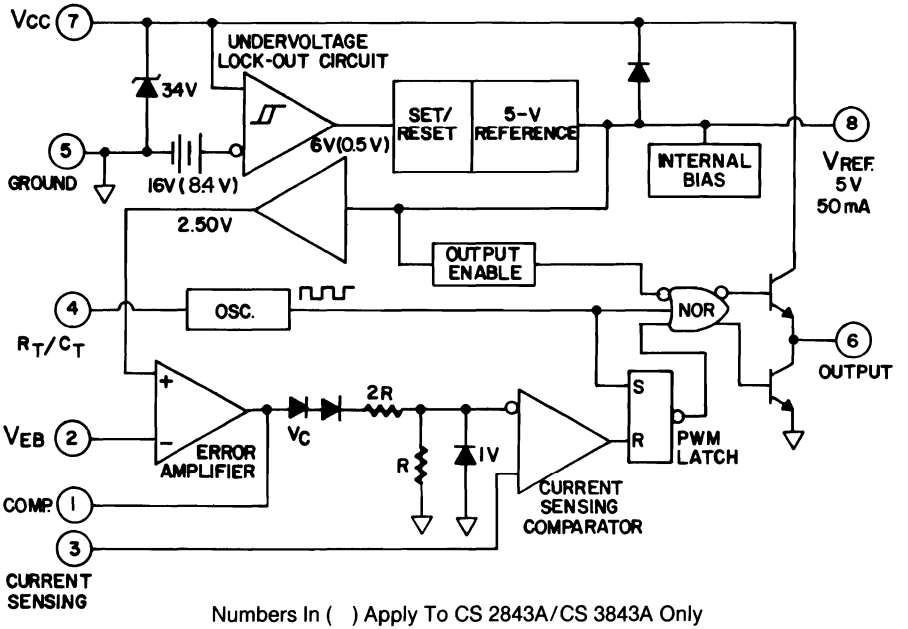
(a) PEAK VS. AVERAGE CURRENT ERROR

(b) $I_{AVG.}$ IS CONSTANT FOR VARYING DUTY CYCLE, (CONSTANT LOAD)

FIGURE 2

CURRENT—MODE CONTROL WITH THE CS-3842A

Figure 3 shows a CS-3842A block diagram containing the basic functions necessary to implement current-mode control. This device will operate from 10V to 30V from a low impedance voltage source or can be current fed if the current is limited to less than 30mA. It is optimized to be driven off the rectified line voltage for start-up, requiring typically a current of only 0.5mA.



Numbers In ( ) Apply To CS 2843A/CS 3843A Only

FIG. 3 CS 3842A/3843A BLOCK DIAGRAM

An auxiliary supply voltage is then normally used when the device is in operation as shown in Figure 4. When operating with a supply voltage between 10V and 16V a bootstrap circuit which provides more than 16V is required for overcoming the device's under-voltage lockout circuit turn-ON threshold. The wide hysteresis band (6V) is provided to accommodate variations in the input voltage to the CS-3842A.

For applications requiring lower UVLO thresholds the CS-3843A can be used. This IC is equivalent to the CS-3842A but with the exception that it will turn ON at 8.4V and turn OFF at 7.9V.

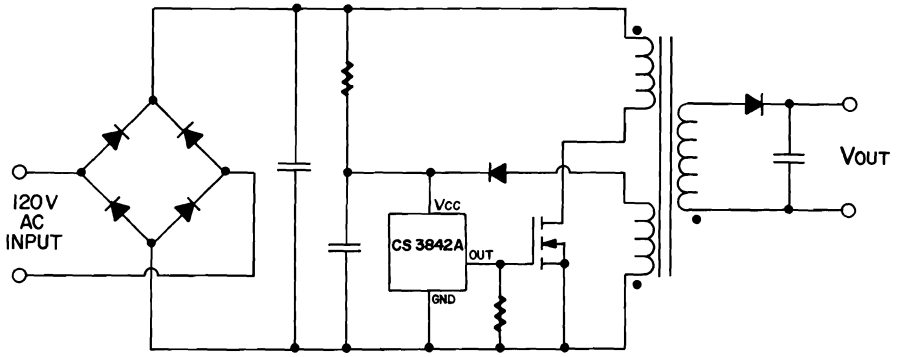


FIG. 4 COMMON OFF-LINE OPERATION OF CS 3842A

THE OSCILLATOR SECTION

After V_{ref} is stabilized the timing capacitor, C_t charges through R_t up to about 2.7V, then discharges down to about 1.1V for every cycle of the oscillator. Since C_t must begin charging from 0 volts instead of 1.1V on the first cycle, the ON time would be longer than in subsequent cycles.

This is objectionable in certain applications so the CS-3842A latches the output to its low state until the end of the first cycle (Figure 5). Another feature in this device regarding the oscillator is that the internal current source which discharges C_t is trimmed to provide an accurate maximum duty cycle clamp without relying on external timers to synchronize the oscillator. The timing components can be selected, not only to set the frequency of the oscillator, but also to set the maximum duty cycle permitted in the power supply topology used.

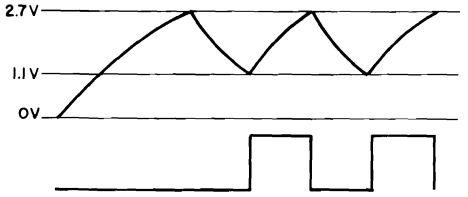


FIG. 5 THE FIRST PULSE IS BLANKED OUT BECAUSE IT EXCEEDS THE MAXIMUM DUTY CYCLE CLAMP

Typical waveforms illustrating the CS-3842A in operation are shown in Figure 6. During the discharge cycle of the R_t/C_t waveform it can be seen how the oscillator internally blanks the output to limit the duty cycle, which is selected by the user. When V_{in} increases, the slope of the switch current (which actually is the combination of the inductor current slope referred to the primary, the transformer magnetizing current, and any slope compensation) also increases such as to provide instant duty cycle correction without using the error amplifier's dynamic range. Next, if a sudden increase in load current occurs the error amplfier shifts the control line to a higher level in order to allow the inductor to conduct more current. Since the rate of change of the current on the inductor is fixed by the voltage applied, if the peak current does not intersect the control line the duty cycle clamp will time out first and prevent the conduction time from exceeding the maximum ON time. Also, since the output voltage drops due to the load increase, the down-slope of the inductor current decreases as well, allowing the current pulse to rapidly converge to a steady state value.

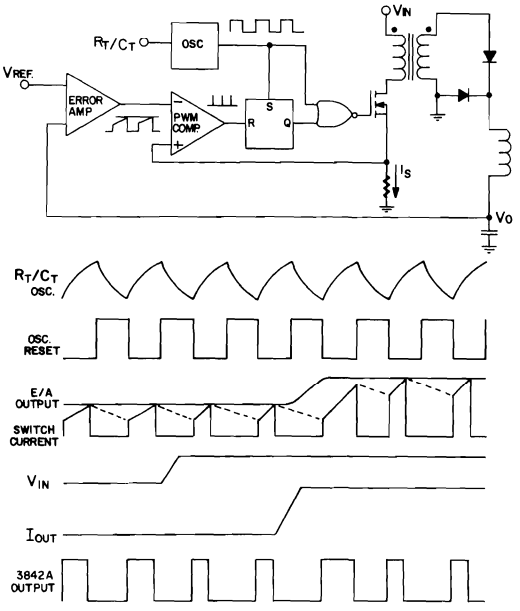


FIG. 6 CS 3842 A TYPICAL WAVEFORMS

APPLYING THE CS-3842A

Combining the high frequency operation of the oscillator with the high current drive capability of the CS-3842A a 500W, 200KHz power supply was designed for this application. Since the CS-3842A has only one output it is solely limited to single ended topologies. A two transistor forward converter was then chosen for this application. Advantages of this topology are: First, the voltage rating for the MOSFETs is reduced to one-half that of a single transistor forward converter. (400V compared to 800V).

Besides, it is unlikely that an 800V, 10A MOSFET be found, and still be cost effective! Second, snubber networks are required only for load line shaping of the MOSFETs. The energy stored in the leakage inductance is effectively returned to the input via clamp diodes. Third, the ripple current rating on the output filter capacitor is less severe than in flyback converters. One notable disadvantage of this topology is the limit on the maximum duty cycle which results in less efficient transformer utilization. The complete schematic of the power supply is shown in Figure 7.

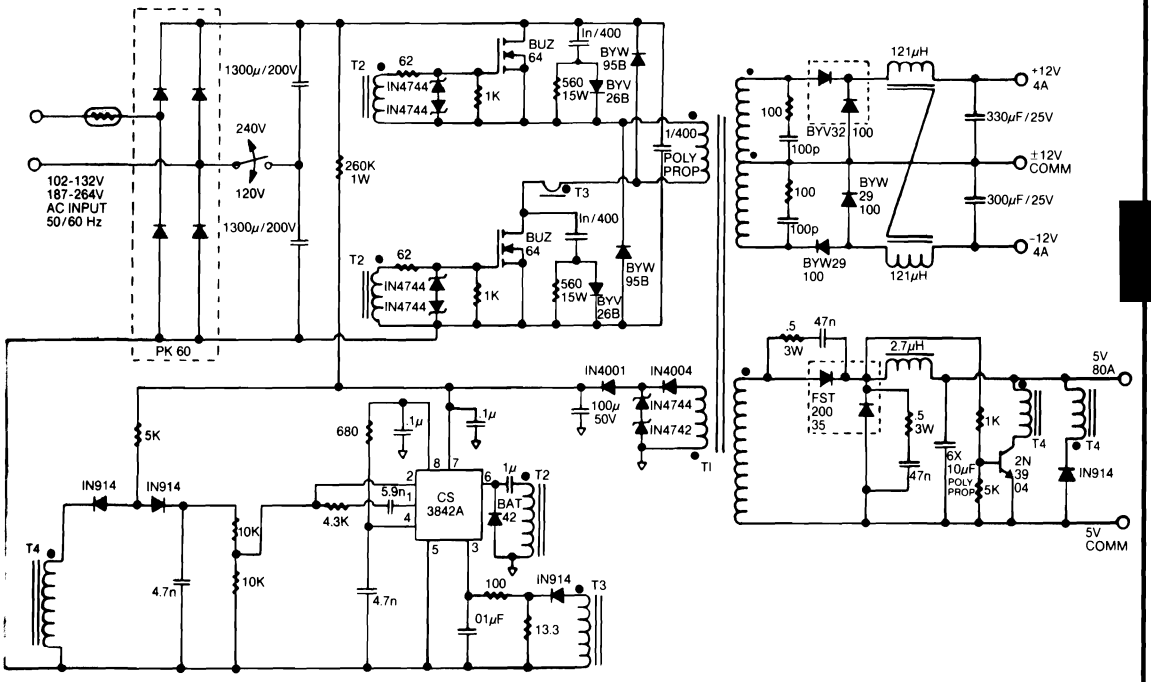


FIGURE 7 SCHEMATIC OF 500W, 200KHz POWER SUPPLY

INPUT SECTION

To determine the required capacitance the input power should be approximately known and this can be done by making an estimate of the power losses expected in the circuit.

Expected Losses	
Schottky diodes: (80A) (.55V)	=44W
Power MOSFETs: Assume 5% of P_o	=25W
Diodes on +12V output. (two diodes conduct at any one time: (.8V)(4A)(2)	=6W
Power Tranformer:	=20W
Inductors: (estimate)	=10W
Snubbers, control ckt, etc:	=20W
Total estimated losses	=125W
Expected Input Power	=625W

Input Capacitance:

Since the AC input voltage is rectified, the capacitors must deliver energy at twice the line frequency.

$$E_{in} = \frac{P_{in}}{2f} = \frac{625}{(2)(60)} = 5.21 \text{ JOULES} \qquad (1)$$

The minimum peak voltage expected is $187\sqrt{2} - 2 = 262V$. The 2V accounts for 2 diode drops on the input bridge. If we assume initially the capacitor valley voltage to be 200V then from

$$E_{in} = \frac{1}{2} C_{eq} (V_{pk}^2 - V_{min}^2) \qquad (2)$$

$$C_{eq} = 364\,\mu f$$

or C=728uf because the two capacitors are in series. Anticipating tolerances and going through some iterations to find a commercially available capacitor that would meet the ripple current requirements two Sprague 1300 uf/200V 36DX series capacitors were selected. The valley voltage is recalculated using Eqn. (2) and found to be 229V.The capacitor conduction time is then determined.

$$t_c = \frac{\cos^{-1}(V_{min}/V_{pk})}{2\pi f} = 1.35\ \text{msec} \qquad (3)$$

The instantaneous maximum capacitor charging current is

$$i_{chg} = C_{eq}(V_{pk} - V_{min})/t_c = 15.9A \qquad (4)$$
$$= I_{pk}$$

Assuming a rectangular shaped charging current pulse, the RMS value is:

$$I_{chg} = I_{pk}\sqrt{2ft_c} = 6.4A \qquad (5)$$

The DC current is

$$I_{dc} = I_{pk}(2ft_c) = 2.58A \qquad (6)$$

Since the DC component of the current is zero in the capacitors, the RMS value of the charging current becomes

$$I_{rms} = \sqrt{I_{chg}^2 - I_{dc}^2} = 5.86A \qquad (7)$$

The discharge current is determined as follows

$$I_{dis} = I_{in}\left(\frac{T}{2} - t_c\right)\frac{2}{T} = \frac{P_{in}}{V_{pk}}\left(\frac{T}{2} - t_c\right)\frac{2}{T}$$
$$= \frac{P_{in}}{V_{pk}}\left(\frac{1}{2f} - t_c\right)2f$$
$$= \frac{P_{in}}{V_{pk}}(1 - 2t_cf) \qquad (8)$$

Substituting in Eqn.(8) the known parameters gives I_{dis}=2A. Now, the total RMS capacitor current is

$$I_{rms_{tot}} = \sqrt{I_{rms}^2 + I_{dis}^2} = 6.19A \qquad (9)$$

The manufacturer's maximum RMS current specified at 85°C and 120Hz is 3.15A, but at less than 55°C this value is multipled by a factor of 2 or 6.30A. This is still acceptable in most commercial applications. Keep in mind that a higher value of capacitance reduces the charging capacitor duty cycle not only increasing the RMS current in the capacitors but also increasing the peak charging current, putting a severe stress on the input rectifiers.

Repeating the above calculations for 50Hz input frequency the RMS current comes out to be 5.92A, which is still within the capacitor's specifications.

The input bridge rectifier must be chosen so it will be able to handle the peak capacitor charging current plus the DC current into the power supply. Surge current limiting during start-up should also be provided.

POWER TRANSFORMER DESIGN

Operating at 200KHz the criteria for core selection is more than simply determining the core winding window area product. Core losses and winding losses due to AC resistance increase with increasing frequency and contribute to a higher temperature rise in the transformer.To analyze these and other factors in selecting the core would be beyond the scope of this paper. The core chosen is a Magnetics Inc. PQ4040, P material. The turns ratio is given by

$$n = \frac{(V_{in(min)} - 2V_T)D_{max}}{V_o + V_L + V_f} \qquad (10)$$

where:

$V_{in\ (min)}$=the minimum dc voltage above which the power supply regulates

V_T=the drain to source ON voltage across a MOSFET at full load.

D_{max}=the maximum duty cycle.

V_o=the output voltage.

V_L=dc resistance voltage drop in the filter choke at FL.

V_f=forward drop across the Schottky diode at FL.

$$n = \frac{(200-6)(.45)}{5+.2+.6} = 15$$

Note that $V_{in(min)}$ is lower than the input capacitor valley voltage in order to provide some hold-up time.

The saturation flux density for P material at high temperature is a little above 3000 Gauss. To prevent core saturation due to a sudden load step increase at high line, and to keep the core losses down, a safe value of 1500G is used. The minimum primary turns for a forward converter is given by

$$N_p > \frac{V_{in(min)} \times 10^8}{2\Delta B_{max} A_e f_s} \qquad (11)$$

where

A_e= effective core area (cm^2)

f_s= switching frequency

$$N_p > \frac{200 \times 10^8}{2(1500)(2.01)(2 \times 10^5)} = 17\ T$$

In order to obtain the right voltages for the number of turns and be able to fit the wire effectively in the bobbin the primary uses 30 turns composed of six #24AWG wires in parallel. The reason for using 5 wires in parallel as opposed to a single larger wire is to reduce the AC resistance in the wires caused by the skin effect. To minimize the primary leakage inductance a split primary was used to completely surround the main secondary. A four turn auxilliary winding of #30AWG was wound on top of the primary, separated by tape, in order to provide good coupling of the primary. This is again repeated in the second primary half and the two auxiliary windings paralleled.

The secondary consists of two turns of two 16-mil copper foil strips 0.9" wide. And finally the ±12 volt secondary is a split 10 turn winding consisting of two #19 AWG wires. Shields were

also placed between the primary and the main secondary to return any noise coupled by parasitic capacitance in the windings. The transformer was also designed to provide adequate line isolation. A summary of the transformer data is as follows:

Winding	Turns
Primary	30
5V secondary	2
±12 secondary	5 each
Auxiliary	4

The auxiliary winding provides power to the CS-3842A once the IC is in operation. The two zener diodes on the auxiliary supply circuit clamp the voltage on the reset cycle to a maximum of 27.8V, which translates to (30/4)(27.8V) = 208.5V on the primary.

To determine the power available at the auxiliary winding the magnetizing current must be calculated first. This is done by determining the primary inductance. For the PQ-4040, P material, the inductance factor, A_L, given is 5020mH/1000 turns. The primary inductance is $5020(30/1000)^2 = 4.5$mH. The magnetizing current is then

$$I_{mag} = \frac{V_{min}\, D_{max}}{L_p\, f_s} = \frac{(200)(.45)}{(4.5 \times 10^{-3})(2 \times 10^5)} = 100\,mA \quad (12)$$

On the auxiliary winding, the current is scaled in proportion to the turns ratio, therefore $I_{aux} = (7.5)(100mA) = 750mA$. Averaging this current over one cycle gives a current of $I_{aux}(1-D_{max})/2 = 200$ mA. If the reset voltage is 27.8V during $(1-D_{max})$, the power available is about 3.15W.

If the control circuit demands more power than that provided by the auxiliary winding the reset voltage will start to drop. To correct this problem a small gap may be placed in the transformer core. If the energy available is more that required by the control circuitry a bleeder resistor should be added to protect the zenor diodes from excessive power dissipation.

OUTPUT FILTER DESIGN

During t_{off} we write a voltage equation around the loop indicated by the current direction in Figure 8.

$$V_L = V_O + V_F = \frac{L\Delta I_L}{t_{OFF}} \quad (13)$$

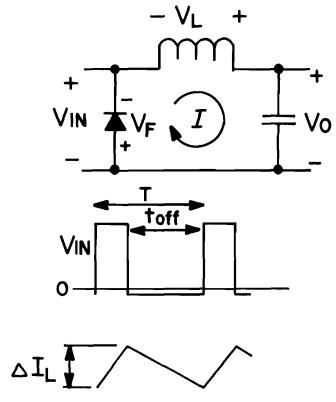


FIG. 8 THE OUTPUT FILTER CIRCUIT.

The maximum OFF time is then determined from the minimum duty cycle.

$$D_{min} = \frac{V_{in(min)}\, D_{max}}{V_{in(max)}} = \frac{194V\,(0.45)}{370V} = 0.23 \quad (14)$$

$$t_{off\,(max)} = (1 - D_{min})\, T_s = 3.85\,\mu sec \quad (15)$$

If we select the inductor current ripple, $\Delta I_L = 8A$ then the value of inductance required is, from equation (13).

$$L = \frac{V_L\, t_{off\,(max)}}{\Delta I_L} = \frac{(5.6)(3.8 \times 10^{-6})}{8} = 2.7\mu H \quad (16)$$

The maximum DC current through the inductor is 80A. From this we determine the LI^2 requirement.

$$L I^2 = (2.7 \times 10^{-6})(80)^2 = 17.3\,mJ \quad (17)$$

This value is helpful in selecting the core size. The core selected here is a Ferroxcube EC-52-3C8. EC cores are very popular because they provide adequate space for large wire sizes which are required for low voltage high current applications. Because the windings are not totally enclosed by the core better cooling is possible.

The required inductance factor can be calculated from

$$A_L = \frac{(BA_e)^2 \times 10^{-4}}{LI^2} \quad (18)$$

For a flux density of 1500 Gauss:

$$A_L = \frac{[(1500)(1.8)]^2 \times 10^{-4}}{17.3} = 42\,mH/1000\ TURNS$$

The ampere-turns required is

$$NI = \frac{10BA_e}{A_L} = \frac{10(1500)(1.8)}{42} = 643\ At \quad (19)$$

dividing by the current the number of turns required is

$$N = 643/80 = 8T$$

The gap required is

$$\ell_g = \frac{4\pi N^2 A_e (10^{-9})}{L} = \frac{4\pi (8)^2 (1.8)(10^{-9})}{2.7 \times 10^{-6}} \quad (20)$$

$$= .536\,cm \text{ or } .211\,in$$

The core can be gapped by grinding down the center post. You can select a gapped core like the EC52G-3C8(2X) which has a 180 mil gap and grind it down to size. Another method would be to put spacers in the outer posts. Since the length of the gap must be made proportional to the cross sectional area of the core where the gap is, a little geometry is required to approximate the area of the outer posts. The following relation can be used to convert the center post gap required, l_g, to the length of an equivalent gap using spacers, l'_g

$$\ell'_g = .3643\ell_g \quad (21)$$

Substituting the value of l_g required we obtain l'_g=77 mils.

To be able to conduct the full load current two strips of 16 mil by 1 inch copper foil was used.

The following formula can be used to calculate the filter capacitance,

$$C = \frac{\triangle I_L}{8 f_s \triangle V_{pp}} \qquad (22)$$

where V_{pp} is the peak-to-peak voltage ripple desired. For this application 80mV was chosen. Therefore

$$C = \frac{8}{8(2 \times 10^5)(.08)} = 62.5\,\mu f$$

The ESR required is:

$$R_{ESR} = \frac{V_{pp}}{I_L} = \frac{0.08}{8} = 10\,m\Omega \qquad (23)$$

Six 10 microfarad polypropylene capacitors are used yielding a combined ESR of 1.5mΩ

CURRENT SENSE CALCULATION

The peak current on the primary is the sum of the peak inductor currents of the secondaries referred to the primary by their turns ratios plus the magnetizing current.

$$I_{pri(pk)} = \frac{84}{15} + 2\left(\frac{4.5}{6}\right) + .1 = 7.2A$$

Allowing a margin on the current limit use 7.5A. Because this current would require a 5 watt current sensing resistor to develop a 1 volt signal amplitude a current transformer was used with a turns ratio of 100.

$$I_{cs} = 7.5/100 = 75\,mA$$

The required current sense resistor becomes

$$R_{cs} = 1/.075 = 13.3\Omega$$

A low pass filter was used to smooth out high frequency noise coupled to the current sense signal.

CLOSED LOOP DESIGN

The zero associated with the capacitor bank ESR is at a frequency of

$$f_{ESR} = \frac{1}{2\pi(1.5 \times 10^{-3})(60 \times 10^{-6})} = 1.77\,MHz$$

The two load resistance extremes in the main output are:

$$R_{o(min)} = 5V/80A = 0.0625\Omega$$

$$R_{o(max)} = 5V/5A = 1\Omega$$

Note that the voltage feedback loop looks only at the 5V output. The output capacitor bank and the load resistance form a moving pole with corner frequencies at

$$f_{p(max)} = \frac{1}{2\pi R_{o(min)} C} = 42\,KHz \qquad (24)$$

$$f_{p(min)} = \frac{1}{2\pi R_{o(max)} C} = 2.65\,KHz \qquad (25)$$

The output-to-control signal is expressed as

$$\frac{V_o}{V_c} = \frac{i_L}{V_c} R_o H_f(S) = \frac{n n' R_o}{3 R_{cs}} \left(\frac{1 + S R_{ESR} C}{1 + S R_o C}\right) \qquad (26)$$

where:

n= primary to second turns ratio

n' current sense transformer turns ratio.

At maximum load

$$\left.\frac{V_o}{V_c}\right|_{f \to 0} = \frac{15(100)(.0625)}{3(13.3)} = 2.35, 7.42\,dB$$

At the minimum load

$$\left.\frac{V_o}{V_c}\right|_{f \to 0} = \frac{15(100)(1)}{3(13.3)} = 37.6, 31.5\,dB$$

For good overall stability, the unity gain loop crossover should be chosen at a frequency less than one-fourth the switching frequency. Selecting the crossover frequency to be 42KHz the error ampliflier is required to provide -7.42dB compensation. The compensation network used is shown in Figure 9. Letting the error amplifier gain cross unity at 2.65KHz good overall gain bandwith product can be acheived combined with adequate phase margin. Calculating the corner frequency for the zero we have.

$$7.42 = -20(\log 2.65 - \log f_z)$$

Solving for f_z we get 6.23KHz

To provide -7.42dB the attenuation ratio should be .4256. From this, C_1 becomes 5.9nF and since R_1=10K then R_2=4.3K. The gain vs frequency response curves are shown in Figure 9.

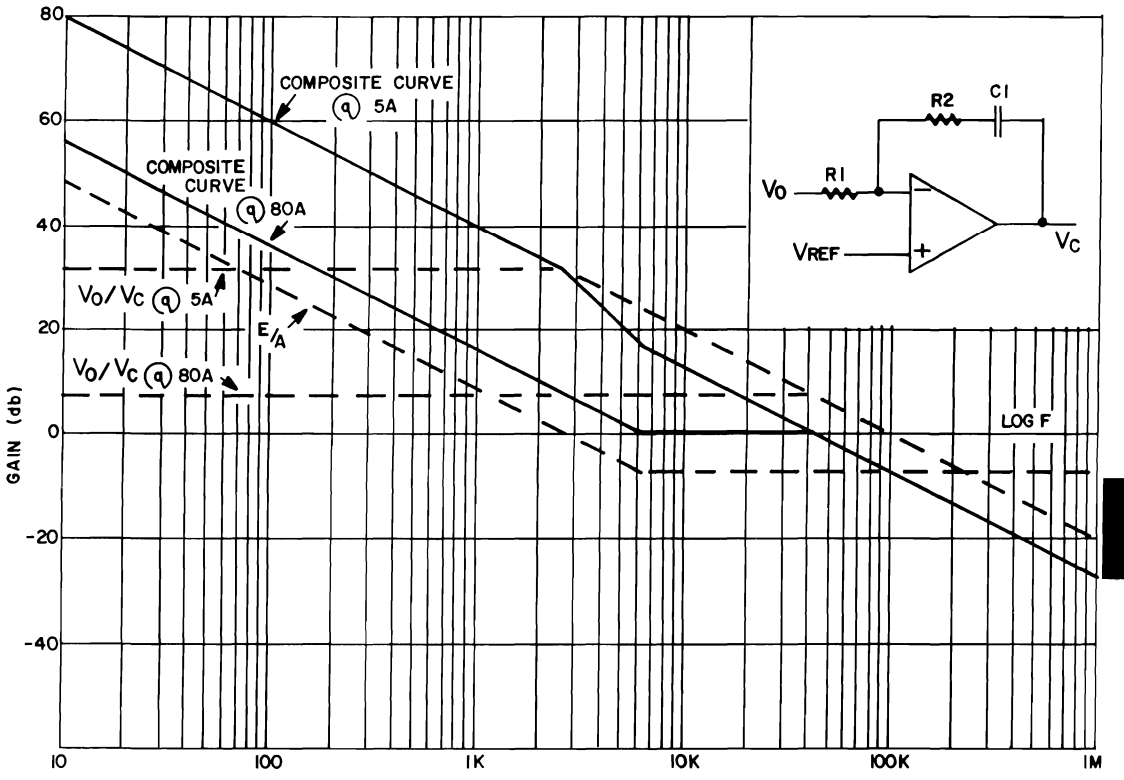


FIG. 9 FREQUENCY RESPONSE DIAGRAM FOR POWER SUPPLY. INSET E/A CONFIGURATION.

To provide isolated output voltage feedback to the error amplifier a small signal transformer, T4, is used. This transformer is switched at 200KHz by using the power transformer's 5V secondary output to drive a transistor. On the secondary of T4 one diode is used to rectify the output while another diode is connected in opposite direction so as to cancel the temperature dependence effect of the forward voltage of the first diode.

OTHER CONSIDERATIONS

When designing high power converters the combined effect of high power with high frequency requires a very careful layout. Identify all the high di/dt paths making them short, and keeping them away from the control circuit.

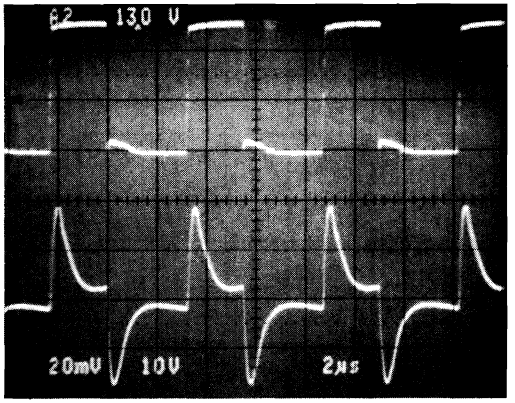
Bypassing of the input DC bus should be done right at the power MOSFETs while low level bypassing should be done at the V_{cc} input of the CS-3842A. The feedback signals, especially the one from the voltage feedback, go to the high impedence input of the error amplifier and can not be bypassed without affecting the amplifier's dynamic performance. The use of a separate low level ground is also recommended, especially of ground plane construction.

When using the CS-3842A to drive inductive loads, as in the case of transformer coupled drive circuits, there is a tendency to drive the output pin below ground, thus interfering with the IC's operation. To correct this problem a low power Schottky diode should be connected from pins 5 to 6 to clamp the output. Another point to keep in mind is that when the oscillator is used also as a maximum duty cycle clamp, the noise on the R_t/C_t should be minimized, again by careful layout of the board.

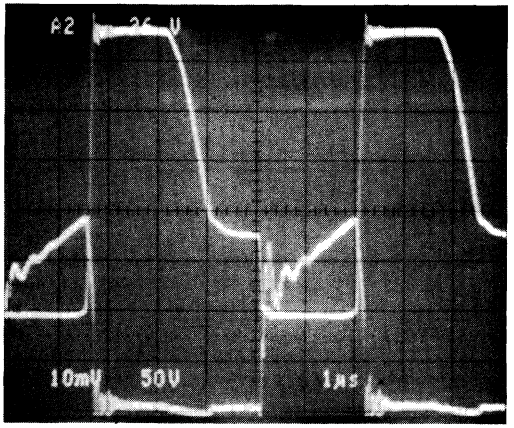
Slope compensation is not required in this application because of less than 50% duty cycle operation and because the filter on current sense signal prevents the turn-ON spike from prematurely tripping the PWM comparator. To be capable of operating efficiently at light loads and also reduce the ripple current on the output capacitors, the inductor current ripple was made small. Shallow inductor current ramps also reduce the peak to average inductor error to a negligible amount.

Figure 10 shows some characteristic waveforms of this power supply.

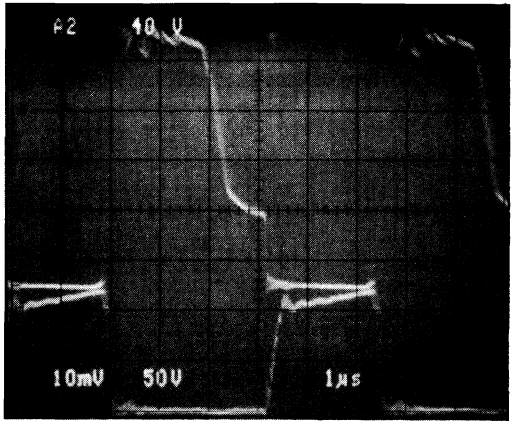
FIGURE 10



(a) CS-3842A OUTPUT VOLTAGE AND CURRENT (200mA/div)



(b) V_{DS}(TOP), I_D(BOT) (.5A/div) LOW LOAD



(c) V_{DS}(TOP), I_D (BOT) (2A/div) HIGH LOAD

MAGNETICS

T1: Core: Magnetics Inc. P-44040-UG
Pri: 30T 6X #24AWG split around main secondary.
Aux: 4T #30AWG in parallel
Sec (5V): 2T 2X .016 X .9 Cu. foil
Sec (+12V): 10T C.T. 2 X #19

T2: Core: Ferroxcube 846XT250-3C8
Pri: 16T #22
Secondaries: 14T #22

T3: Core: Ferroxcube 768XT188-3E2A
Pri: IT
Sec: 100T, #32

T4: Core: Ferroxcube 768XTI88-3E2A
Pri: 8T #27
Sec: 8T #27
Ter: 4T #27

LI: Core: Ferroxcube EC52-3C8
Winding: 8T 2X .016 X 1 Cu. foil
77 mil gap on all three posts

L2: Core: Ferroxcube 2616PA250-3B7
Winding: 22T 5X (2 #27 in parallel)

REFERENCES

B. Holland, "Modeling, Analysis and Compensation of the Current Mode Converter" Proceedings of Powercon 11, Paper I-2, 1984

C. Deisch "Simple Switching Control Method Changes Power Converter Into a Current Source" **PESC '78 Record** (IEEE Publication 78CH1337-AES), pp 300-306.

CSC™ CHERRY SEMICONDUCTOR

CS-2844/CS-3844
CS-2845/CS-3845

CURRENT MODE PWM CONTROL CIRCUIT

DESCRIPTION

The CS-3844/45 provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS-3844 family incorporates a new precision temperature-controlled oscillator to minimize variations in frequency. An internal toggle flip-flop, which blanks the output off every other clock cycle, limits the duty-cycle range to less than 50%. An under-voltage lockout ensures that V_{REF} is stabilized before the output stage is enabled. In the CS-2844/CS-3844 turn on occurs at 16V and turn Off at 10V. In the CS-2845/CS-3845 turn on is at 8.4V and turn Off at 7.6V.

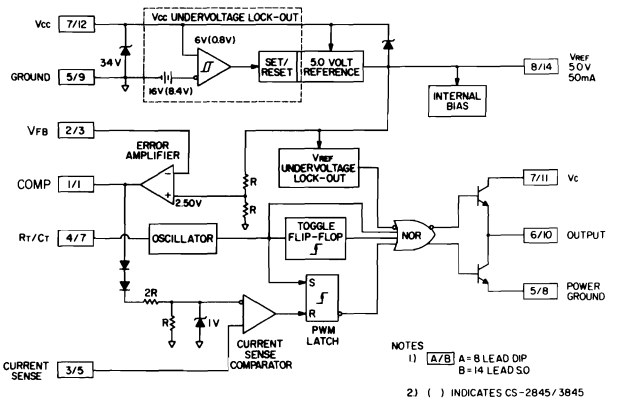
Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as gate of a power MOSFET. The output is low in the off state, consistent with N-channel devices.

ORDERING INFORMATION

PART NO.	0°C to 70°C	-25° to 85°C	PACKAGE
CS-3844N	*		8L PDIP
CS-3844D	*		14L SO
CS-3844DW	*		16L SO WIDE
CS-2844N		*	8L PDIP
CS-2844J		*	8L CDIP
CS-2844DW		*	16L SO WIDE

PART NO.	0°C to 70°C	-25° to 85°C	PACKAGE
CS-3845N	*		8L PDIP
CS-3845D	*		14L SO
CS-3845DW	*		16L SO WIDE
CS-2845N		*	8L PDIP
CS-2845J		*	8L CDIP
CS-2845DW		*	16L SO WIDE

BLOCK DIAGRAM

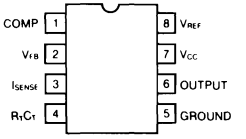


FEATURES:

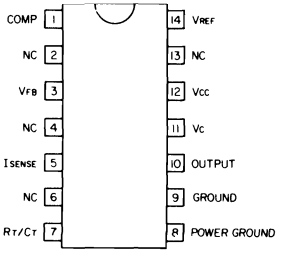
- Optimized for off-line control
- Temperature compensated oscillator
- 50% maximum duty-cycle clamp
- V_{REF} stabilized before output stage is enabled
- Low start-up current
- Pulse-by-pulse current limiting
- Improved U/V lockout
- Double pulse suppression
- 1% trimmed bandgap reference
- High current totem pole output

PIN CONNECTIONS

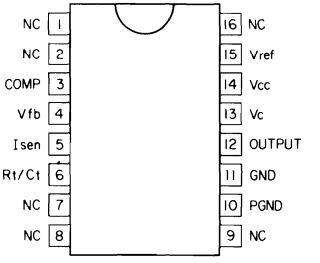
DIP/CDIP



SO-14



SO-16



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{CC}<30mA) ..... Self Limiting
Supply Voltage (Low Impedence Source) 30V
Output Current ..... ±1A
Output Energy (Capacitive Load) 5μJ
Analog Inputs (V_{FB}, V_{SENSE}) ..... -0.3V to 5.5V
Error Amp Output Sink Current 10mA

ELECTRICAL SPECIFICATIONS: Unless otherwise stated, specifications apply for -25≤Ta≤85°C for CS-2844/2845, 0≤Ta≤70°C for CS-3844/3845. Vcc=15V (Note 1); R_T=10K, C_T=3.3nf for sawtooth mode.

PARAMETER	TEST CONDITIONS	CS-2844 CS-2845			CS-3844 CS-3845			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j=25°C, I_{REF}=1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12≤V_{IN}≤25V		6	20		6	20	mV
Load Regulation	1≤I_{REF}≤20mA		6	25		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	4.82		5.18	V
Output Noise Voltage	10Hz≤f≤10kHz, T_j=25°C (Note 2)		50			50		μV
Long Term Stability	T_A=125°C, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit	T_A=25°C	-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	Sawtooth Mode, T_j=25°C	47	52	57	47	52	57	kHz
Voltage Stability	12≤V_{cc}≤25V		0.2	1		0.2	1	%
Temp. Stability	Sawtooth Mode T_{MIN}≤T_A≤T_{MAX} (Note 2)		5			5		%
Amplitude	V_{OSC} (peak-to-peak)		1.7			1.7		V
Error Amp Section								
Input Voltage	V_{COMP}=2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	V_{FB}=0V		-0.3	-1		-0.3	-2	μA
A_{VOL}	2≤V_O≤4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
PSRR	12≤V_{CC}≤25V	60	70		60	70		dB
Output Sink Current	V_{FB}=2.7V, V_{COMP}=1.1V	2	6		2	6		mA
Output Source Current	V_{FB}=2.3V, V_{COMP}=5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	V_{FB}=2.3V, R_L=15K to ground	5	6		5	6		V
V_{OUT} Low	V_{FB}=2.7V, R_L=15K to V_{REF}		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	V_{COMP}=5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12≤V_{CC}≤25V (Note 3)		70			70		dB
Input Bias Current	V_{SENSE}=0V		-2	-10		-2	-10	μA
Delay to Output	T_j=25° (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=200mA	12	13.5		12	13.5		V
Rise Time	T_j=25°C, C_L=1nF (Note 2)		50	150		50	150	ns
Fall Time	T_j=25°C, C_L=1nF (Note 2)		50	150		50	150	ns
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	V_{FB}=V_{SENSE}=0V R_T=10K, C_T=3.3nF		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC}=25mA		34			34		V
PWM Section								
Maximum Duty Cycle		46	48	50	46	48	50	%
Minimum Duty Cycle				0			0	%

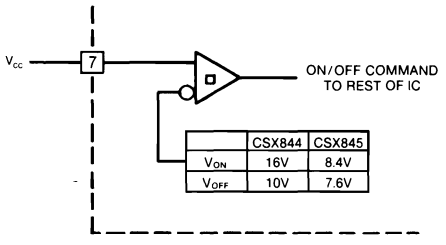
Notes: 1 Adjust V_{CC} above the start threshold before setting at 15V
2 These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{FB}=0.
4. Gain defined as:

$$A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}} ; 0 \leq V_{SENSE} \leq 0.8V.$$

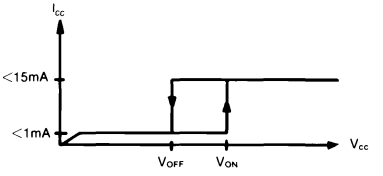
ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	CS-2844			CS-3844			CS-2845 CS-3845			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section											
Start Threshold		15	16	17	14.5	16	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9	10	11	8.5	10	11.5	7.0	7.6	8.2	V

UNDER-VOLTAGE LOCKOUT



	CSX844	CSX845
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Fig. 1

3844/3845 TIMING DIAGRAM

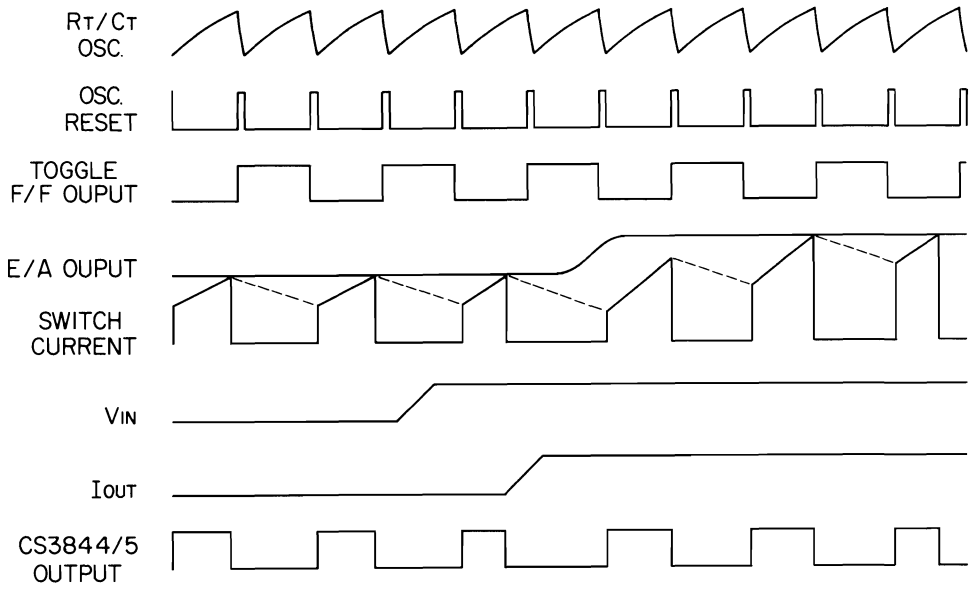


Fig. 2

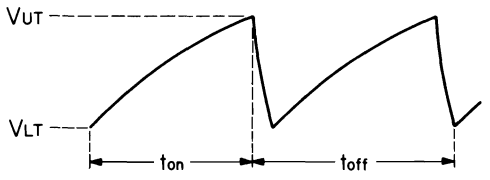
NOTES ON CS-3844 TIMING DIAGRAM

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current. An increase in V_{IN} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of R_T/C_T components.

APPLICATION INFORMATION

Charge and discharge times are determined by the general formulas:



$$t_c = R_T C_T \ell n \left(\frac{V_{REF} - V_{LT}}{V_{REF} - V_{UT}} \right)$$

$$t_d = R_T C_T \ell n \left(\frac{V_{REF} - I_d R_T - V_{UT}}{V_{REF} - I_d R_T - V_{LT}} \right)$$

$t_{on} = t_c$
$t_{off} = t_c + 2t_d$

Assuming typical values for the parameters in the above formulas:

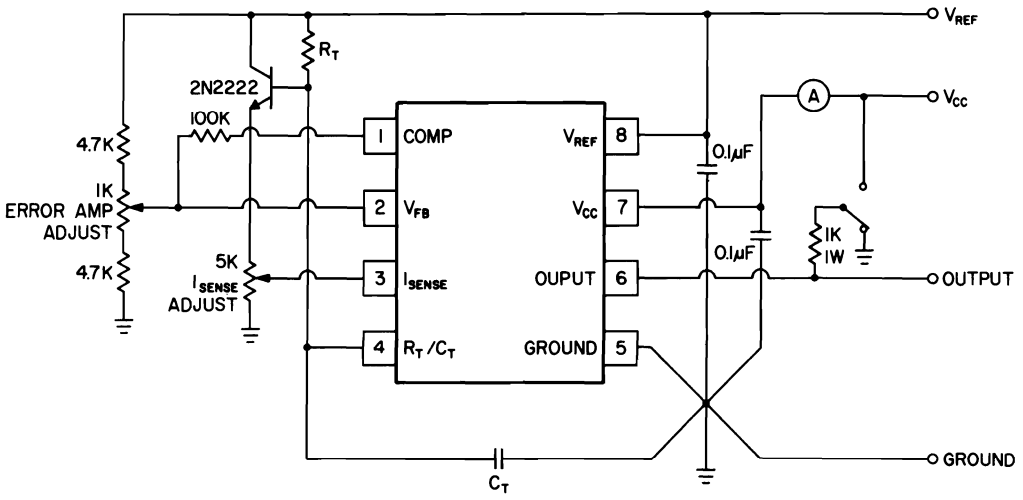
V_{REF}=5.0V, V_{UT}=2.7V, V_{LT}=1.0V, I_d=8.3mA, then

$t_c \approx .5534\ R_T C_T$

$$t_d = R_T C_T \left[\ell n \left(\frac{2.3 - .0083 R_T}{4.0 - .0083 R_T} \right) \right]$$

For better accuracy R_T should be $\geq$ 10KΩ.

OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

THERMAL RESISTANCE (P_d MAX = (T_j - T_a) / Thermal Resistance, where T_j = 155°C)

PACKAGE		Pd MAX VALUES		
	Thermal Resistance °C Watt	CSX84X Pd Max @ 25°C (mW)	CS384X Pd Max @ 70°C (mW)	CS284X Pd Max @ 85°C (mW)
8LDIP	90	1444	944	778
8LCERDIP	90	1444	944	778
14LSO Narrow	130	1000	654	
16LSO Wide	95	1368	895	

TYPICAL AND MAXIMUM POWER DISSIPATION BY SECTION

Supply Current (Voltage Fed Mode):
P_d TYP = V_{cc} TYP (I_{cc} TYP) = 15V (.012A) = 180mW
P_d MAX = V_{cc} MAX (I_{cc} MAX) = 30V (.017A) = 510mW

Supply Current (Current Fed Mode):
P_d TYP = V_{cc} TYP (I_{cc} TYP) = 34V (.025A) = 850mW
P_d MAX = V_{cc} MAX (I_{cc} MAX) = 40V (.03A) = 1200mW

Output:
P_d TYP = V_{sat} TYP (I_{out} TYP sink or source) 25% DC = 1.5V (.2A) (.25) = 75mW
P_d MAX = V_{sat} MAX (I_{out} MAX sink or source) 50% DC = 2.2V (.2A) (.5) = 220mW

Reference (Voltage Fed Mode):
P_d TYP = (V_{cc} TYP - V_{ref} TYP) I_{ref} TYP = (15V - 5V) .01A = 100mW
P_d MAX = (V_{cc} MAX - V_{ref} MIN) I_{ref} MAX = (30V - 4.9V) .03A = 753mW

TOTAL TYPICAL POWER DISSIPATION

Conditions:
V_{cc} = 15V, I_{ref} = 10mA, I_{out} sink or source = 200mA, DC = 25%
P_d TYP TOTAL = (180 + 75 + 100)mW = 355mW

TOTAL MAXIMUM POWER DISSIPATION (Voltage Fed Mode)

Conditions:
V_{cc} = 30V, I_{ref} = 30mA, I_{out} sink or source = 200mA, DC = 50%
P_d MAX TOTAL = (510 + 220 + 753) = 1483mW

CSC™ CHERRY SEMICONDUCTOR

CS-3865

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

DESCRIPTION

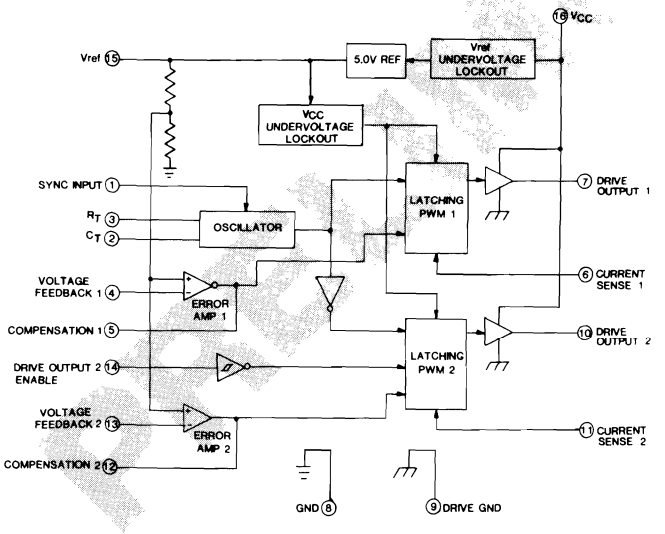
The CS-3865 is a high performance, fixed frequency, dual current mode controller. It is specifically designed for Off-Line and DC to DC converter applications offering the designer a cost effective solution with minimal external components. This integrated circuit features a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, drive output 2 enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering of each output.

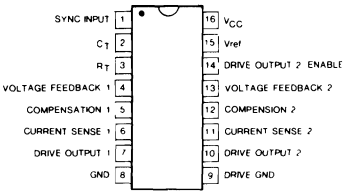
FEATURES:

- Unique oscillator for precise duty cycle limit and frequency control
- Current mode operation to 500 kHz
- Automatic feed forward compensation
- Separate latching PWMs for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- Drive output 2 enable pin
- Two high current totem pole outputs
- Input undervoltage lockout with hysteresis
- Low start-up and operating current

BLOCK DIAGRAM



PIN CONNECTIONS



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Total power supply and zener current	($I_{CC}+I_Z$)	50	mA
Output current, source or sink (Note 1)	I_O	1.0	A
Output energy (capacitive load per cycle)	W	5.0	μJ
Current sense, enable and voltage Feedback inputs	V_{in}	-0.3 to +5.5	V
Sync input —High state (voltage)	V_{IH}	5.5	V
—Low state (reverse current)	I_{IL}	-5.0	mA
Error amp output sink current	I_O	10	mA

Parameter	Symbol	Value	Units
Power dissipation and thermal characteristics			
DW suffix package SO-16			
Maximum power dissipation @ T_A=25°C	P_D	862	mW
Thermal resistance junction to air	RθJA	145	°C/W
N suffix package			
Maximum power dissipation @ T_A=25°C	P_D	1.25	W
Thermal resistance junction to air	RθJA	100	°C/W
Storage temperature range	T_{stg}	-65 to +150	°C
Operating junction temperature	T_J	+150	°C
Operating ambient temperature		0 to +70	°C

ELECTRICAL CHARACTERISTICS: (V_{CC} = 15V [Note 2] , R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	(I_O = 1.0mA, T_J = 25°C)	V_{ref}	4.9	5.0	5.1	V
Line Regulation	(V_{CC} = 11V to 15V)	Reg_{line}	—	2.0	20	mV
Load Regulation	(I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	25	mV
Total Output Variation over Line, Load and Temperature		V_{ref}	4.85	—	5.15	V
Output Short Circuit Current		I_{SC}	30	100	—	mA
Oscillator and PWM Sections						
Total Frequency Variation over Line and Temperature	(V_{CC} = 11V to 15V, T_A = T_{low} to T_{high})	f_{OSC}	46.5	49	51.5	kHz
Frequency Change with Voltage	(V_{CC} = 11V to 15V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	%
Duty Cycle at each Output	—Maximum	DC_{max}	46	49.5	52	%
	—Minimum	DC_{min}	—	—	0	
Sync Input Current	—High State (V_{in} = 2.4V)	I_{IH}	—	170	250	μA
	—Low State (V_{in} = 0.8V)	I_{IL}	—	80	160	
Error Amplifiers						
Voltage Feedback Input	(V_O = 2.5V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current	(V_{FB} = 5.0V)	I_{IB}	—	-0.1	-1.0	μA
Open-Loop Voltage Gain	(V_O = 2.0 to 4.0V)	A_{VOL}	65	100	—	dB
Unity Gain Bandwidth	(T_J = 25°C	BW	0.7	1.0	—	MHz
Power Supply Rejection Ratio	(V_{CC} = 11V to 15V	PSRR	60	90	—	dB
Output Current	—Source (V_O = 3.0V, V_{FB} = 2.3V)	I_{Source}	-0.45	-1.0	—	mA
	—Sink (V_O = 1.2V, V_{FB} = 2.7V)	I_{Sink}	2.0	12	—	
Output Voltage Swing	-High State (R_L=15k to ground, V_{FB}=2.3V)	V_{OH}	5.0	6.2	—	V
	-Low State (R_L=15k to V_{ref}=2.7V), VF	V_{OL}	—	0.8	1.1	
Current Sense Section						
Current Sense Input Voltage Gain	(Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold	(Note 4)	V_{th}	430	480	530	mV
Input Bias Current		I_{IB}	—	-2.0	-10	μA
Propagation Delay	(Current Sense Input to Output)	$t_{PLN(IN/OUT)}$	—	150	300	ns
Drive Output 2 Enable Pin						
Enable Pin Voltage						V
High State	(Output 2 Enabled)	V_{IH}	3.5	—	V_{ref}	
Low State	(Output 2 Disabled)	V_{IL}	0	—	1.5	
Low State Input Current	(V_{IL} = 0V	I_{IB}	100	250	400	μA
Drive Outputs						
Output Voltage						V
Low State	I_{Sink} = 20mA	V_{OL}	—	0.1	0.4	
	I_{Sink} = 200mA		—	1.6	2.5	
High State	I_{Source} = 20mA	V_{OH}	13	13.5	—	
	I_{Source} = 200mA		12	13.4	—	
Output Voltage with UVLO Activated	(V_{CC} = 6.0V, I_{Sink} = 1.0mA	V_{OL} (UVLO)	—	0.1	1.1	V
Output Voltage Rise Time	(C_L = 1.0nF)	t_r	—	28	150	ns
Output Voltage Fall Time	(C_L = 1.0 nF)	t_f	—	25	150	ns

Notes: 1. Maximum package power dissipation limits must be observed
2. Adjust V_{CC} above the Start-Up threshold before setting to 15V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} = 0°C T_{high} = +70°C

4. This parameter is measured at latch trip point with V_{fb} =0V.
5. Comparator gain is defined as.

$$A_V = \frac{\Delta \text{ V Compensation}}{\Delta \text{ V Current Sense}}$$

ELECTRICAL CHARACTERISTICS: (V_{CC} = 15V [Note 2] , R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].) (Cont'd.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Undervoltage Lockout Section						
Start-Up Threshold		V_{th}	13	14	15	V
Minimum Operating Voltage After Turn-On		V_{CC} (min)	9.0	10	11	V
Total Device						
Power Supply Current		I_{CC}				mA
Start-Up	(V_{CC} = 12V)		—	0.6	1.0	
Operating	(Note 2)		—	20	25	
Power Supply Zener Voltage	(I_{CC} = 30mA)	V_Z	15.5	17	19	V

Notes: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C T_{high} = +70°C
4. This parameter is measured at latch trip point with V_{fb} =0V.
5. Comparator gain is defined as:

$$A_V = \frac{\Delta \text{ V Compensation}}{\Delta \text{ V Current Sense}}$$

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

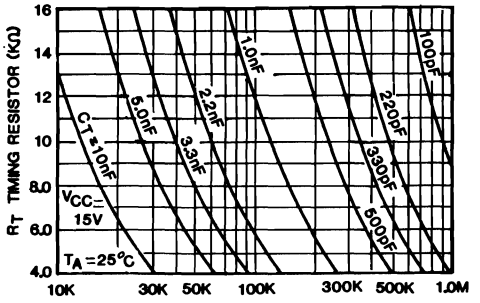


FIGURE 2 — MAXIMUM OUTPUT DUTY CYCLE versus OSCILLATOR FREQUENCY

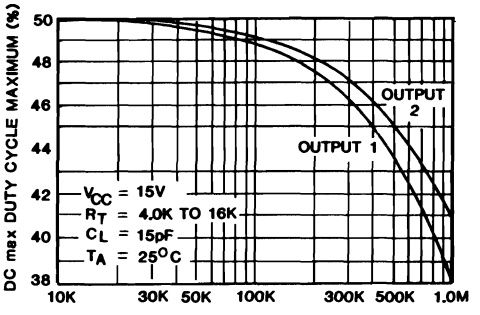


FIGURE 3 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

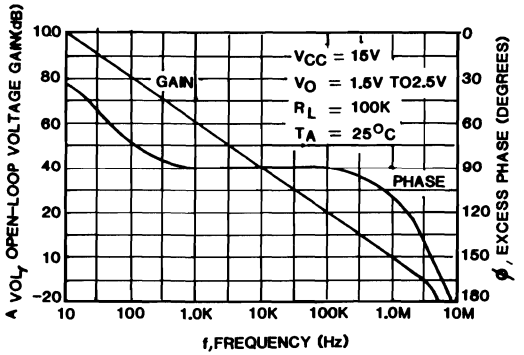


FIGURE 4 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

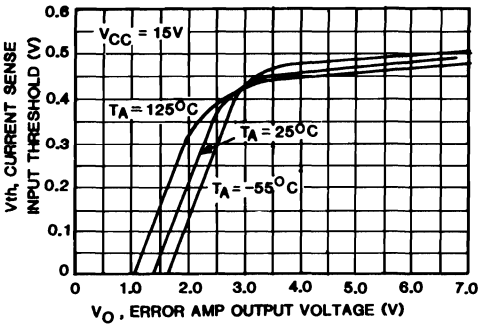


FIGURE 5 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

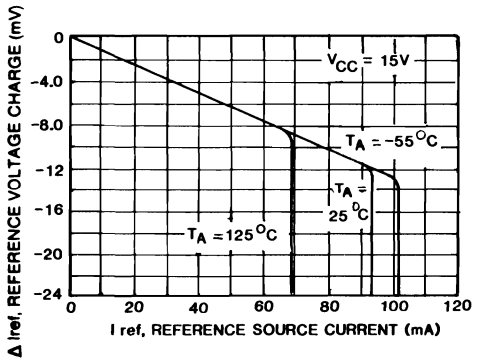


FIGURE 6 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

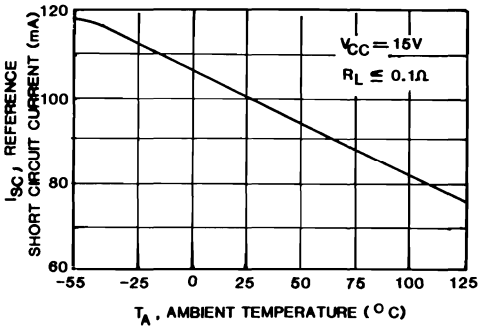


FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

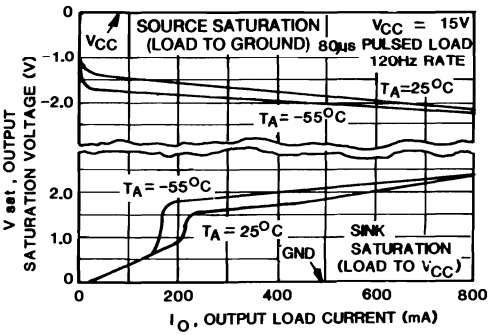
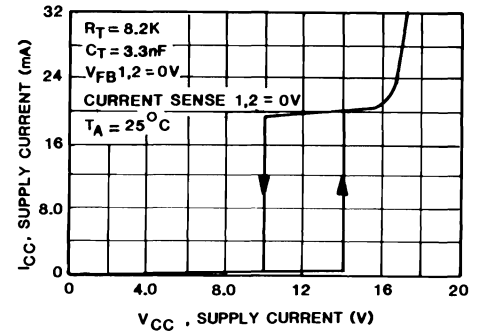


FIGURE 8 — SUPPLY CURRENT versus SUPPLY VOLTAGE



4

OPERATING DESCRIPTION

The CS-3865 is a high performance, fixed frequency, dual channel current mode controller specifically designed for Off-Line and DC to DC converter applications. This device offers the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 9. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lockout circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5V and 1.6V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0kΩ to 16kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on-time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 10, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved.

OPERATING DESCRIPTION (Cont'd.)

Error Amplifier

Each channel contains a fully-compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71 degrees of phase margin (Figure 3). The non-inverting input is internally biased at 2.5V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum inout bias current is -1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5,12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval.

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_f\,(MIN) \approx \frac{3.0\,(0.5V) + 1.4V}{0.5\ mA} = 5800\ \Omega$$

Current Sense Comparator and PWM Latch

The CS-3865 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator-PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(PIN\ 5,\ 12)} - 1.4V}{3R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5V. Therefore the maximum peak switch current is:

$$I_{pk}\,(max) = \frac{0.5V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk\ (max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability.

FIGURE 9 — REPRESENTATIVE BLOCK DIAGRAM

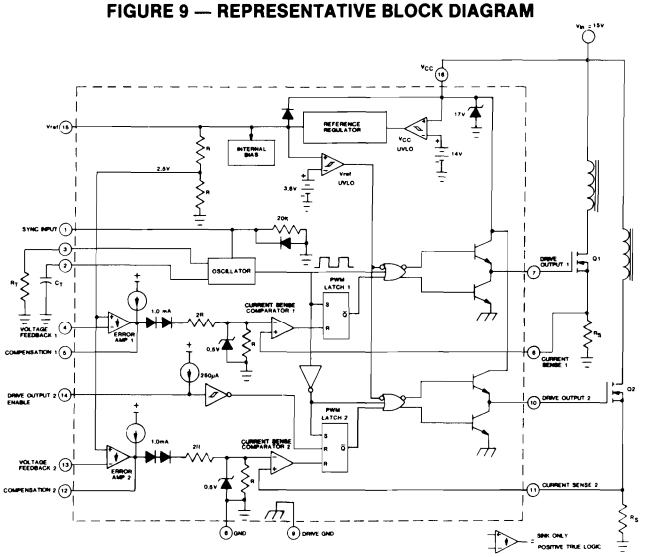
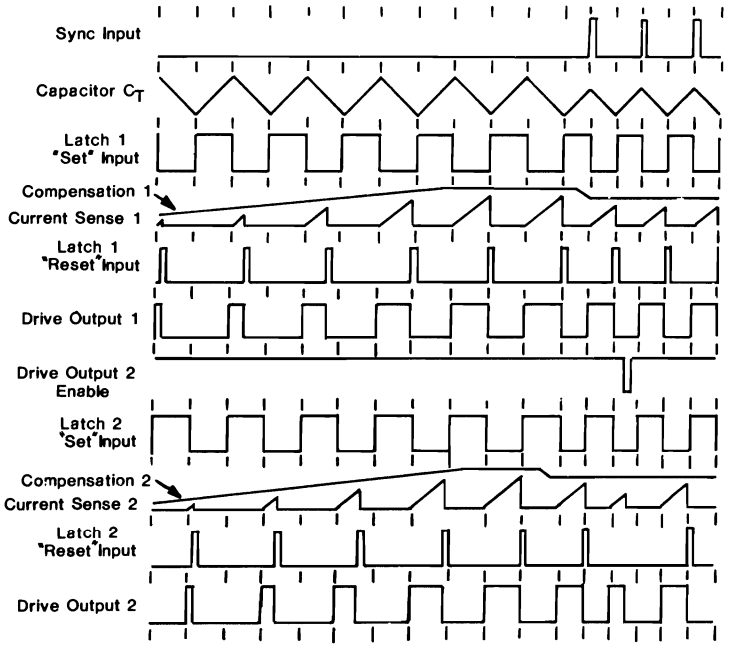


FIGURE 10 — TIMING DIAGRAM



4

OPERATING DESCRIPTION (Cont'd.)

Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC} and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14V and 10V respectively. The hysteresis and low start-up current makes these devices ideally suited to off-line converter applications where efficient bootstrap start-up techniques are required. The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6V and 3.4V. A 17V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system start-up. The guaranteed minimum operating voltage after turn-on is 11V.

Drive Outputs and Drive Ground

Each channel contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. The Drive Outputs are capable of up to ±1.0A peak current and have a typical rise and fall time of 28 ns with a 1.0nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull-down resistor. Cross-conduction current in the totem-pole output stage has been minimized for high speed operation. The average added power due to cross-conduction with V_{CC} = 15V is only 60mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFET's, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off. The outputs do not contain internal current limiting, therfore an external series resistor may be required to prevent the peak output current from exceeding the ±1.0A maximum rating. The sink saturation (V_{OL}) is less than 0.4 at 100mA

A separate Drive Ground pin is provided and, with proper implementation, will signifigantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk\ (max)}$ clamp level.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

Reference

The 5.0V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30mA for powering any additional control system circuitry.

OPERATING DESCRIPTION (Cont'd.)

Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feed-back inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage-divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

PIN FUNCTION DESCRIPTION

Pin #	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will sychronize the Oscillator. A DC voltage within the range of 2.4V to 5.5V will inhibit the Oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free-running Oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0k and 16k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction od output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0A are sourced and sinked by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0A are sourced and sinked by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin in the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after start-up is 11V to 15.5V.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-3865N	16 Lead PLASTIC DIP
CS-3865DW	16 Lead SO WIDE

CSC™ CHERRY SEMICONDUCTOR

CS-360

ONE MEGAHERTZ RESONANT-MODE CONTROL

DESCRIPTION

The CS-360 integrated circuit controller is designed for use in resonant and quasi-resonant mode topologies. The architecture is configured to allow operation in the following variable frequency control methods: Fixed ON-Time, Fixed OFF-Time, and a combination of Fixed ON/OFF Times.

It contains the standard complement of "house-keeping" functions, including a programmable UVLO, soft-start, and current limiting.

The precision Voltage-Controlled Oscillator is specifically designed to offer a high degree of linearity (typ. 2%) over a frequency range of 100KHz to 1MHz, while accurately clamping the minimum and maximum frequency to user selected values. Control of the output driver "deadtime" is externally programmable with a single resistor.

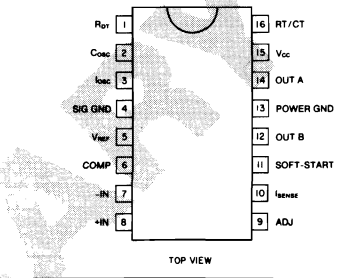
The temperature-compensated One-Shot delivers a well-controlled pulse width to the dual 1A Totem-Pole output drivers and is retriggerable, allowing it to function in the three different control methods.

FEATURES:

- 1 MHz VCO with user programmable min/max frequencies
- Temperature-Compensated One-Shot
- Programmable Output "Deadtime"
- UVLO with low start-up current and alternative start/stop thresholds
- Latched over-current protection
- Soft-start

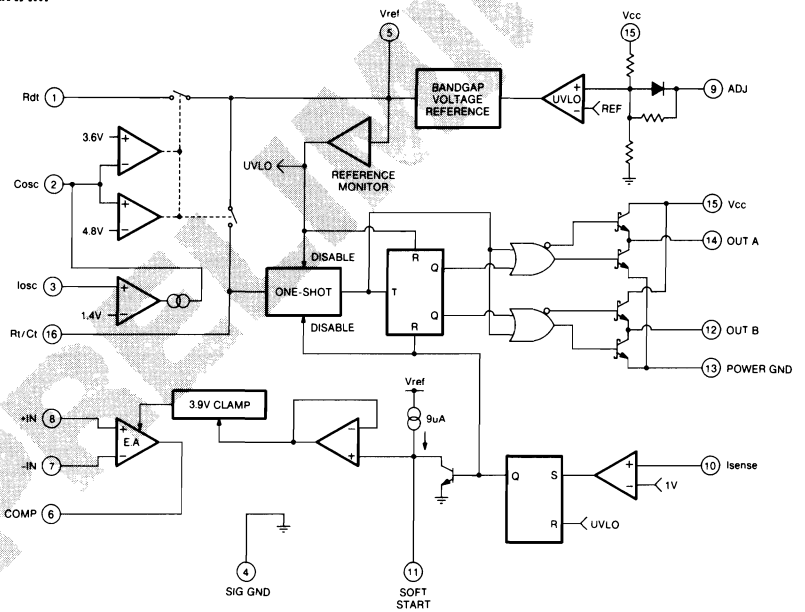
4

PIN CONNECTIONS



TOP VIEW

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	Rating	Units
Power Supply Voltage (V_{cc})	20	V
Output Current, Source or Sink		
DC	0.3	A
Pulse (0.5 μS)	1.5	A
Error Amplifier Input Voltage	-1 to 6	V
Current Sense Input Voltage	-1 to 6	V
ADJ pin (UVLO) Input Voltage	-1 to VCC	V
Reference Output Current	10	mA
Power Dissipation (TA = 50°C)	1	W
Junction Temperature	150	°C
Storage Temperature	-55 to 125	°C
Lead Temperature (Soldering, 10S)	300	°C

RECOMMENDED OPERATING CONDITIONS:

PARAMETER	PIN	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	15		10	12	18	V
Load Capacitance	12, 14		—	1.2	2.5	nF
Error Amplifier Input Voltage	7,8		1.5	—	5.5	V
One-Shot Timing Resistor (RT)	16		5.0	20	50	KΩ
One-Shot Timing Capacitor (CT)	16		200	300	500	pF
Oscillator Timing Cap. (Cosc)	2		200	300	2000	pF
Oscillator Dead Time Res. (RDT)	1		0	0.3	10	KΩ
Oscillator Frequency	2		0.01	—	1.0	MHz
Ambient Temperature Commercial			0	—	70	°C
Ambient Temperature Industrial			-25	—	85	°C

ELECTRICAL CHARACTERISTICS (Unless specified otherwise: V_{CC} = 12V, C_{osc} = 300pF, T_a = -25 to 85°C for the Industrial version and T_a = 0 to 70°C for the Commercial version.)

PARAMETER	PIN	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Section						
Output Voltage	5	T_a = 25°C I_o = 1mA	5.0	5.1	5.2	V
Line Regulation	5	10V < V_{cc} < 20V		5.0	20	mV
Load Regulation	5	1 < I_o < 10mA		5.0	20	mV
Temp. Stability	5	(Note 1) (O < TA < 70°C)		20	50	mV
Total Output Variation	5	Line, Load, Temp.	4.9		5.3	V
Output Short Circuit	5	T_a = 25°C V5 = 0V	20		100	mA
Error Amp. Section						
Input Offset Voltage	7,8	V7 = 2.5V, V6 = V7			15	mV
Input Bias Current	7,8	V7 = V8 = 2.5V		-0.3	-1.0	uA
Input Offset Current	7,8	V7 = V8 = 2.5V		0.1	1.0	uA
AVol	6		65	90	—	dB
Common Mode Voltage Range	1,2		1.5		5.5	V
Output Sink Current	6		1.0			mA
Output Source Current	6		2.0	5.0		mA
Gain Bandwidth Product	6	(Note 1)	2.5	4.0		MHz
V_{out} Low	6		—	0.7	1.1	V
V_{out} High	6		3.5	3.9	4.3	V
VCO Section Note: R_{MIN} = 95.3KΩ, R_{dt} = 0, C_{osc} = 300pF, R_{osc} = 5620Ω, T_A = 25°C Unless otherwise noted						
Minimum Frequency	2	Error Amplifier Output Low	90	100	110	KHz
Freq. Variation W/VCC, Temp.	2	Error Amplifier Output Low (O<TA<70°C)	85	—	115	KHz
Maximum Frequency	2	Error Amplifier Output Hiigh	900	1000	1100	KHz
V_{peak}	7	R_{dT} = 1KΩ		4.8		V
V_{valley}	7	F_{osc} = 100 KHz		3.6		V
$V_{deadtime}$	1	I1=1mA V2=3.3V		5.1		V
Iosc Pin Input Voltage	3	I3 = 445uA	1.3	1.4	1.5	V
Deadtime Minimum	2	R_{dt} = 0Ω	—	70	100	nS
Deadtime Long	2	R_{dt} = 1KΩ	500	600	700	nS
Deadtime Adjustment Range	2		0.1	—	2.5	uS
One-Shot Section Note: C_t = 300pF, R_{dt} = 1K, T_a = 25°C						
Period Short	12,14	R_t = 14, 3KΩ	1.43	1.5	1.57	uS
P_d Short, Total Variation with V_{cc}, Temp.	12,14	R_t = 14, 3KΩ (O<TA<70°C)	1.40	1.5	1.60	uS
Period Long	12,14	R_t = 47.5KΩ	4.6	5.0	5.4	uS
Setting Range	12,14		0.5	—	10	uS

NOTE 1: Although guaranteed, these parameters are not 100% tested in production.

ELECTRICAL CHARACTERISTICS cont'd.(Unless specified otherwise: V_{CC} = 12V, C_{osc} = 300pF, T_a = -25 to 85°C for the Industrial version and T_a = 0 to 70°C for the Commercial version.)

PARAMETER	PIN	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Section						
Output Low Level	12,14	I_{sink} = 20mA		0.25	0.4	V
		I_{sink} = 200mA		1.5	2.2	V
Output High Level	12,14	I_{sink} = 20mA	18	18.5		V
		I_{sink} = 200mA	117.5	18		V
Output Sink Compliance	12,14	VCC = 6V I12 = I14 = 1mA		1.0	1.5	V
Rise Time	11,14	T_a = 25°C C1 = 1nF (Note 1)		30	60	nS
Fall Time	11,14	T_a = 25°C C1 = 1nF (Note 1)		30	60	nS
Current-Limit Section						
Current-Limit Threshold	10		0.95	1.0	1.05	V
Input Bias Current	10		—	1.0	10	uA
Delay to Output	10	50mV Overdrive	—	70	100	nS
Soft Start Section						
Charge Current	11		4.50	9.0	14	uA
Discharge Current	11		0.7	2.0		mA
Under-Voltage Lockout Section						
Start Threshold	15	Pin 9 open	14.5	16	17.5	V
Stop Threshold	15	Pin 9 Open	8.0	9.0	10	V
Start Threshold	15	Pin 9 = Pin 15	8.0	9.0	10	V
Stop Threshold	15	Pin 9 = Pin 15	7.6	8.6	9.6	V
Vref UVLO Threshold	5		3.7	4.2	Vref	V
Chip Disable Threshold	9		—	—	6.0	V
Adj. Pin Input Current	9	V9 = 0V	—	200	500	uA
Total Supply Current						
Operating (CL = 1nF, Fosc = 500KHz)	15		—	25	35	mA
Start-Up (UVLO Active)	15	Pin 9 = Pin 15	—	0.3	0.6	mA

4

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 1 — SUPPLY CURRENT vs SUPPLY VOLTAGE

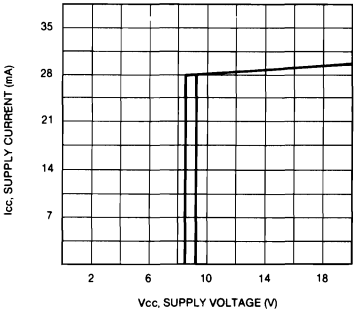


FIGURE 2 — REFERENCE VOLTAGE CHANGE vs REFERENCE CURRENT

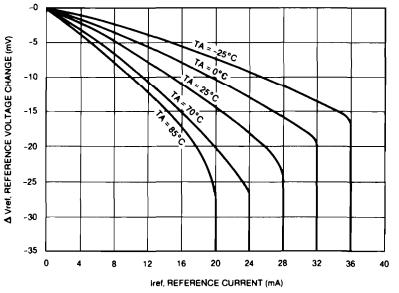


FIGURE 3 — SHORT CIRCUIT CURRENT vs AMBIENT TEMPERATURE

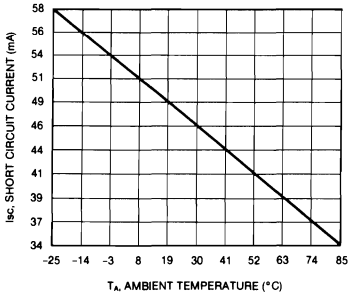
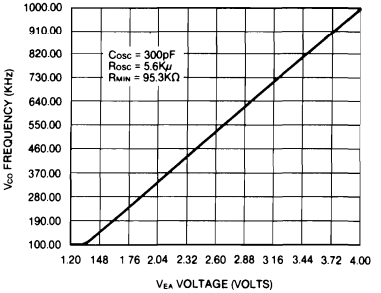


FIGURE 4 — V_{CO} FREQUENCY vs ERROR AMPLIFIER V_{OUT}



TYPICAL PERFORMANCE CHARACTERISTICS cont'd.

FIGURE 5 — MINIMUM CLAMPED FREQUENCY vs MINIMUM TIMING RESISTOR

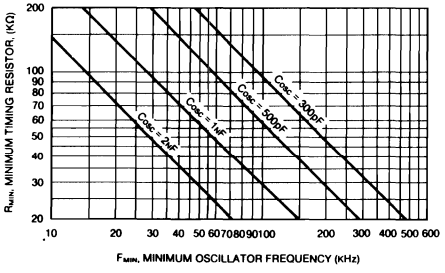


FIGURE 6 — MAXIMUM CLAMPED FREQUENCY vs TIMING CAPACITOR

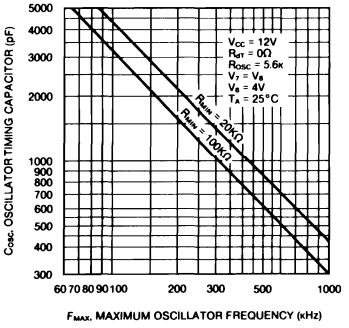


FIGURE 7 — ONE-SHOT PULSE WIDTH vs TIMING RESISTOR

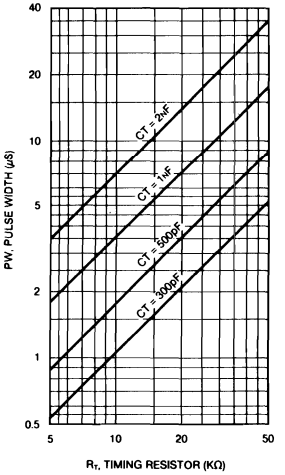
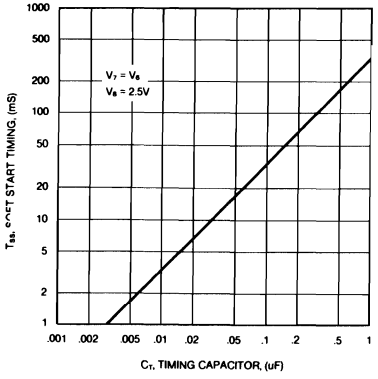


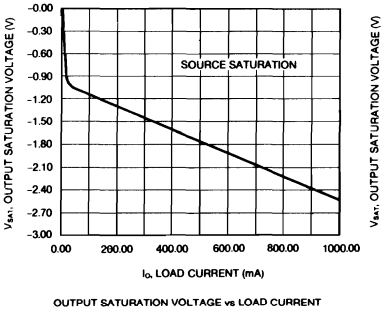
FIGURE 8 — SOFT START TIMING vs TIMING CAPACITOR



SOFT START TIMING vs TIMING CAPACITOR

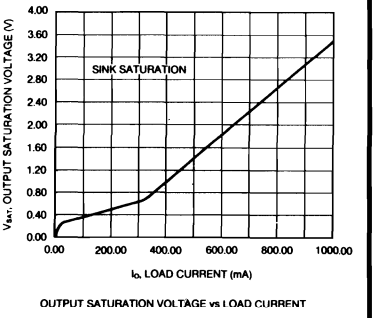
Note: Soft Start Timing is defined as the time required for the error amplifier output voltage to reach 2.5V upon start up.

FIGURE 9 — OUTPUT SATURATION VOLTAGE vs LOAD CURRENT



OUTPUT SATURATION VOLTAGE vs LOAD CURRENT

FIGURE 10 — OUTPUT SATURATION VOLTAGE vs LOAD CURRENT



OUTPUT SATURATION VOLTAGE vs LOAD CURRENT

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-360	16L PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-3805A

RESONANT MODE POWER SUPPLY CONTROLLER

DESCRIPTION

The CS-3805A, which employs fixed on-time, variable frequency control, is specifically intended for resonant mode power supply control applications. Two complementary outputs are capable of directly driving power MOSFETs.

Opening a normally grounded control pin puts the CS-3805A into single-ended operation. In this mode the frequency is doubled and the two outputs are identical so they can be paralleled for increased drive capability.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed.

ABSOLUTE MAXIMUM RATINGS

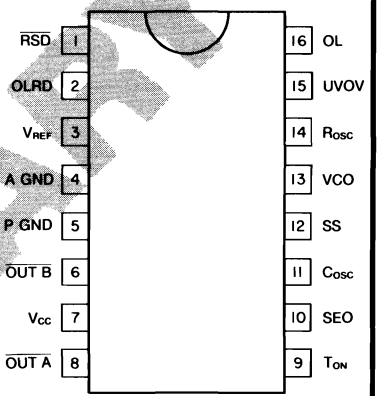
Parameter	Values & Units
Supply Voltage	20V
Undervoltage/Overvoltage Input	-0.4V to 6V
Overload Input	-0.4V to 6V
Remote Shutdown	-0.4V to V_{cc}
VCO Input	-0.4V to V_{cc}
Operating Temperature Range: CS-3805A	$0°C \leq T_A \leq 70°C$
Storage Temperature Range	$-65°C \leq T_S \leq +150°C$
Lead Temperature (Soldering, 10 sec.)	260°C
Junction Temperature	150°C
Power dissipation at $T_A \leq 70°C$	720mW
(derate 9mW/°C for $T_A > 70°C$)	

FEATURES:

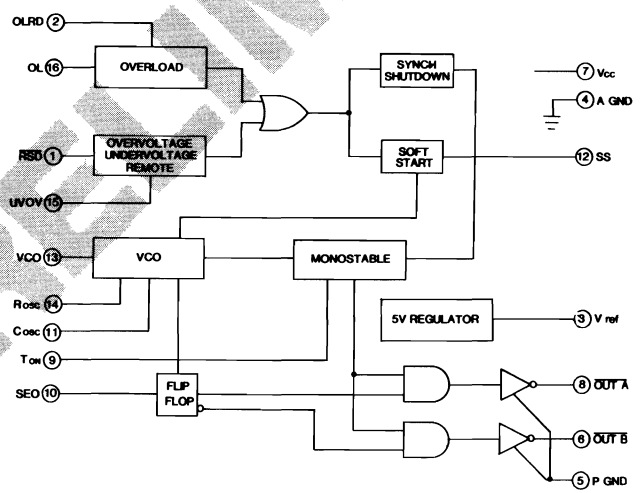
- 1 MHz maximum operating frequency
- Synchronous overload shutdown with delayed restart
- Synchronous overvoltage, undervoltage and remote shutdown
- Soft start
- Single ended or complementary outputs
- Drives power MOSFETs directly (0.8A peak)

4

PIN CONNECTIONS



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Limits apply over 0°C ≤ T_A ≤ 70°C for the CS-3805A with V_{cc} = 12 V. Typical values are at T_A = 25°C. Parameters marked with a * are valid only at T_A = 25°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Internal Vcc Undervoltage Threshold		8.5	9.0	9.5	V
Threshold Hysteresis		—	5	—	%
Supply Current	Undervoltage condition	18	22	24	mA
Voltage Controlled Oscillator					
Maximum Frequency	Single output Complementary output	— —	2 1	— —	MHz MHz
Tolerance of $f$max Tolerance of $f$min	fig. 6 fig. 5	— —	— —	±5 ±20	% %
Tolerance coefficient $f$max Tolerance coefficient $f$min		-300 400	-600 700	-900 1000	ppm/°C ppp/°C
Dead Time T_{OFF}*		—	200	300	ns
Operating Range of VCO Input (Pin 13)	max min	— —	6.5 1.1	— —	V V
Linearity of the VCO		—	—	±5	%
Internal Pull-up Resistor (Pin 13)		8	10	12	kΩ
Output Pulse Width T_{ON} Tolerance		—	—	±5	%
Temperature Coefficient of T_{ON}		0	400	800	ppm/°C
Output Section					
Output Risetime	100pF II 100kΩ load on	—	20	40	n sec
Output Falltime	$\overline{OUT}$ A, $\overline{OUT}$ B	—	15	30	n sec
Output Mismatch	$\overline{OUT}$ A vs $\overline{OUT}$ B, Pin 10 SEO open	—	5	15	n sec
Output Low Level (sink)	$\overline{OUT}$ A & $\overline{OUT}$ B 20mA	—	—	0.7	V
	200mA	—	—	2.2	V
Output High Level (source)	$\overline{OUT}$ A & $\overline{OUT}$ B -20mA	—	—	Vcc-2	V
	-200mA	—	—	Vcc-2.2	V
Reference Section					
Output Voltage *		4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Max Current Capability		—	10	—	mA

ELECTRICAL CHARACTERISTICS continued

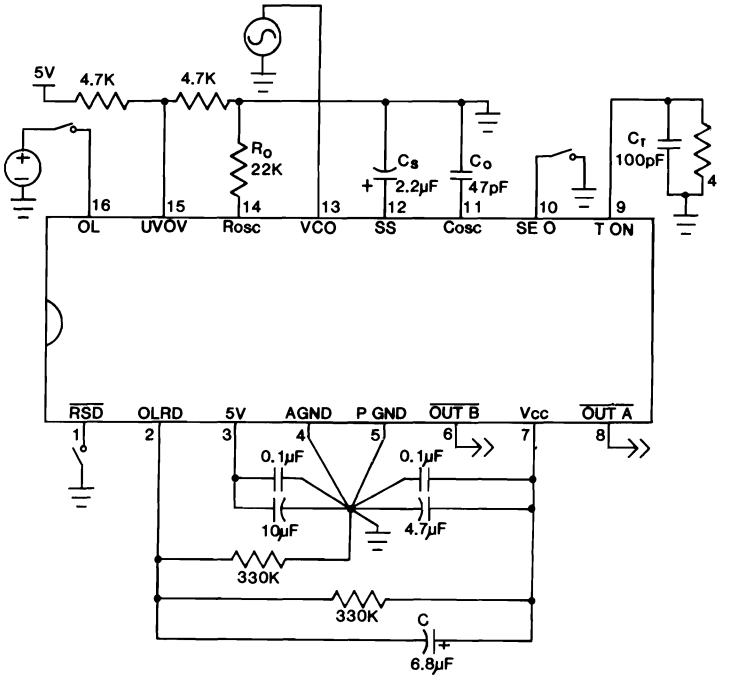
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Section					
Soft-start[1]	C_s = 2.2µF, VCO = 7V	16	19	22	ms
Overload Restart Delay	2R = 330kΩ, C = 6.8µF	1.0	1.3	1.6	sec
Propogation Delay to Shutdown[2]		—	200	300	n sec
Remote Shutdown[3]	Enabled	Vcc-0.8	—	—	V
	Disabled	—	—	3	V
Overload Shutdown (OL) Threshold*		2.7	3.0	3.3	V
OL Threshold Temp. Coefficient		-400	100	500	1ppm/°C
OL Hysteresis		—	3	—	%
OL Trigger Pulse Width		500	—	—	n sec
OL input current Range		-1	—	+15	µA
Overvoltage Threshold* Lockout		2.7	3.0	3.3	V
Undervoltage Threshold* Lockout		1.7	1.9	2.1	V
Temp. Coeff. of Threshold Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		—	3	—	%
Input Current Range (Pin 15)		-1	—	+22	µA

[1] Soft-start time is measured from output enable at minimum frequency to time at which maximum frequency is reached.

[2] If the shutdown Input is triggered at greater than 200ns before the start of the next pulse the pulse will not occur. If there is a shutdown input occurring at less than 200ns before the start of the next pulse, the following pulse is completed in full before the output is disabled.

[3] Refer to pin description for current required.

OPEN LOOP TEST CIRCUIT



Thermal Impedance

16 pin DIL Plastic Package	θ JC	—	42	—	°C/W
16 pin DIL Plastic Package	θ CA	—	70	—	°C/W
16 pin SOIC	θ JA	—	112	—	°C/W

TYPICAL PERFORMANCE CURVES OF THE CS-3805A

For all graphs, Vcc = +12 volts DC and T_A = 25°C. The curves shown below represent typical batch sampled results.

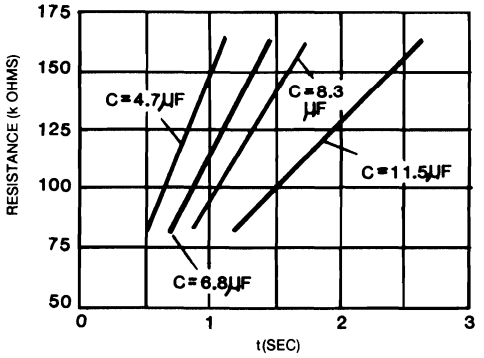


Fig. 1 Overload Restart Delay

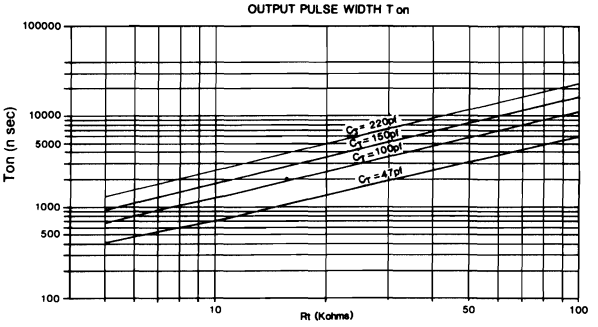


Fig. 2. Output Pulse Width

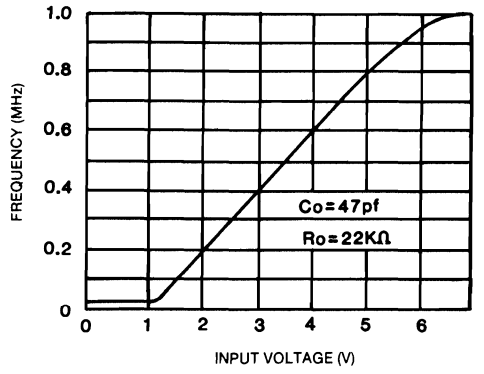


Fig. 3 VCO Frequency vs Input Voltage

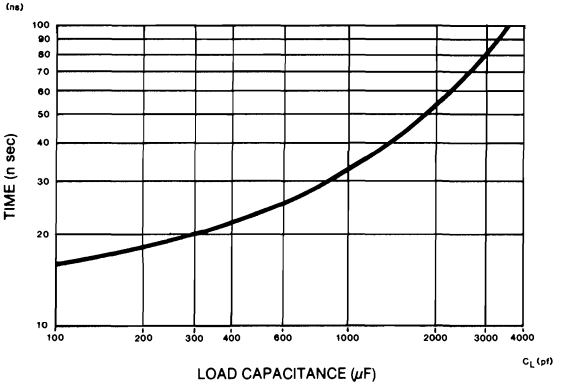


Fig. 4. Output Risetime/Falltime

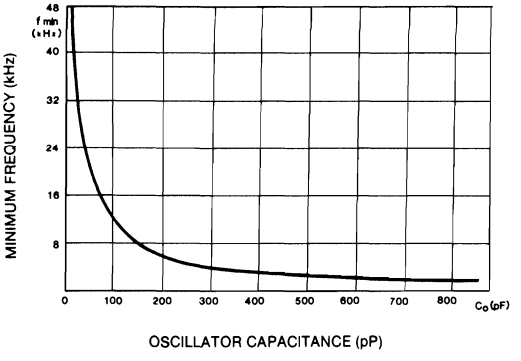


Fig. 5 Minimum Operating Frequency

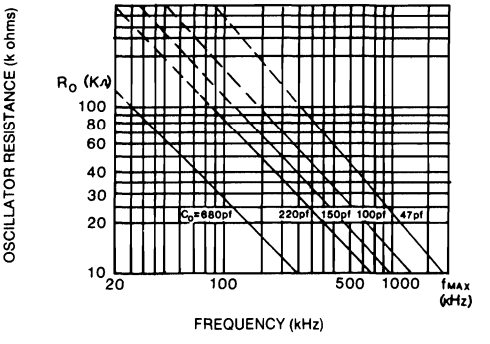


Fig. 6. Maximum Operating Frequency

PIN FUNCTIONS

Pin 1 (RSD) - Remote Shutdown
A low on pin 1 shuts down the CS-3805A. When the pin is released the CS-3805A goes into soft-start. This pin is normally driven by an open collector transistor where the current is given by:

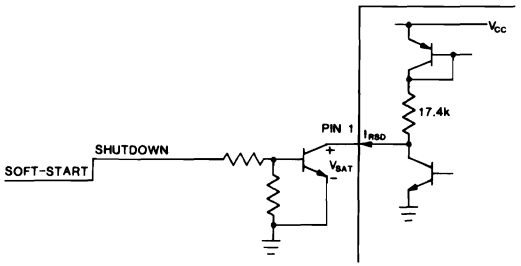


Fig. 7

$$I_{\overline{RSD}} = \frac{(V_{CC} - V_{SAT} - 0.7)V}{17.4\ k\Omega} \quad mA \pm 20\%$$

For CMOS or bipolar circuitry, the configuration may be:

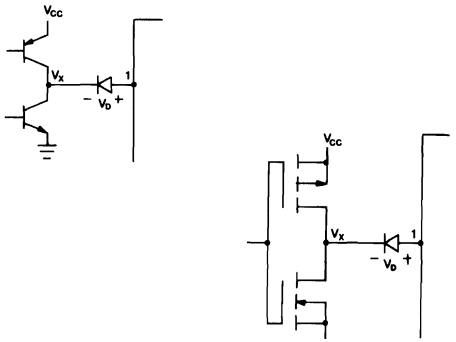


Fig. 8

In all cases the voltage must pull up to a minimum of

$$V_x = V_{cc} - 0.8V$$

assuming diode voltage $V_D \approx 0.4V$ when it is off (non-conducting). If remote shutdown is not used. leave pin 1 open.

PIN 2 (OLRD) - Overload Restart Delay
A 330 kΩ + 330kΩ voltage divider in combination with a 6.8μF capacitor generates a 1.3 second shutdown to restart delay every time the overload sense (pin 16) is activated. Timing starts when the overload is removed; upon timeout soft-start begins. Refer to Figure 1 to select RC combinations for other delays.

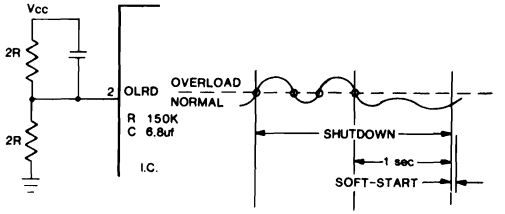


Fig. 9

Pin 3 (5V) - 5V Reference
This is a 5% tolerance regulator used to power most of the internal circuitry. To improve noise rejection it is recommended to decouple this pin with a 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor.

Pin 3 can be used as a reference for any external circuitry as long as the load is less than 10 mA.

Pin 4 (A GND) - Analog Ground
Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and the reference.

Pin 5 (P GND) - Power Ground
Only the output transistors are connected to the power ground, to minimize interference with the logic circuitry.

A GND and P GND are not connected inside the package. Supply decoupling should be done at the connection point of these grounds.

Pin 6 ($\overline{OUT\ B}$) - Output B
Output B is an active low output driver, where the low duration (pulse width) is T_{ON}. It is complementary to pin 8 ($\overline{OUT\ A}$).

Pin 7 (V_{cc}) - Supply Voltage
The power supply trace must be decoupled as close to pin 7 as possible. Currents of 0.5 A levels may be drawn by the CS-3805A. Minimum recommended decoupling is with a 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor.

Pin 8 ($\overline{OUT\ A}$) - Output A
Output A is an active low output driver, where the low duration (pulse width) is T_{ON}, and is complementary to pin 6.

Pin 9 (T_{ON}) - Pulse Width
The constant pulse width T_{ON} is set by a resistor R_T and capacitor C_T. This relationship is shown in Figure 2. R_T + C_T should have a temperature coefficient of -500 ppm/°C for best stability and fall within the following ranges:

$$5\ k\Omega \leq R_T \leq \text{no limit}$$
$$47\ pF \leq C_T \leq 100nF$$

The R_T and C_T should be connected as close as possible to A GND to minimize ground noise variations. The upper limit on pulse width is determined by chip-to chip variation, power supply and component tolerances. The worst case combination must give $T_{ON} < 1/f_{max} - T_{OFF}$, where T_{OFF}=200ns typ. (300ns max.). The off period is required by design of the CS-3805A. The pulse width T_{ON} should be set to give an off period greater than T_{OFF} so that the circuit will operate correctly at f_{max}, where f is the actual operating frequency. Rewriting the equation as:

$$T_{OFF} = 1/f - T_{ON}$$

The CS-3805A will divide the output frequency by two when T_{OFF} decreases to 200ns. This is a failsafe feature to ensure the pulse width will never be incorrect by limiting f_{max}. Under normal operation f_{max} should be limited using R_{OSC}.

Pin 10 (SEO) - Single Ended Output

This pin is normally grounded for complementary outputs in push-pull applications. Opening pin 10 results in a single ended output at double the frequency. $\overline{OUT\ A}$ and $\overline{OUT\ B}$ can then be shorted together for increased drive capability.

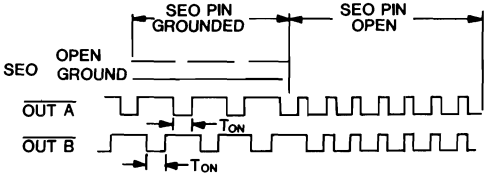


Fig. 10

Pin 11 (C_{OSC}) - Oscillator Capacitor

The capacitor C_{OSC} on this pin, controls the minimum frequency f_{min} of the VCO operating range. Refer to Figure 5 for selection. Layout is critical for this component, keeping leads as short as possible and connecting close to the A GND pin.

Pin 12 (SS) - Soft-Start

A capacitor C_S on this pin provides a controlled start up from f_{min} to f_{max}. The delay is approximately t_{ss} (ms) $\approx 8.7\ C_s$ (μF) for $C_s$between zero and 47μF.

To ensure a full soft-start duration when soft-start is caused by an undervoltage or overvoltage fault, it is necessary to have the fault present for about half the soft-start time.

Pin 13 (VCO) - Voltage Controlled Oscillator Input

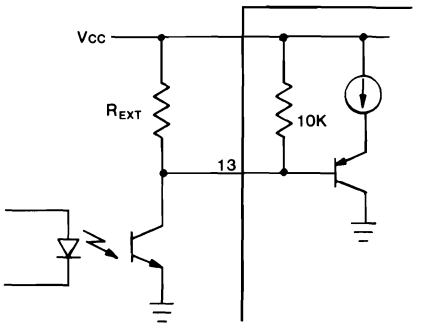


Fig. 11

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 10 kΩ pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Figure 3. The linear input range is from 1.1V to 6.5V where 1.1V represents f_{min} and 6.5V represents f_{max}.

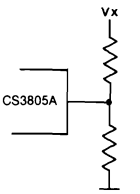
Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor R_{OSC} on this pin, controls f_{max}, the maximum frequency of the VCO operating range. C_{OSC} the capacitor controlling f_{min} must be selected first, then refer to Figure 6 for selection of R_{OSC}. For good stability, a 1% resistor with a temperature coefficient of -600 ppm/°C, is recommended. Minimum value for R_{OSC} is 10kΩ.

Pin 15 (UVOV) - Undervoltage/Overvoltage

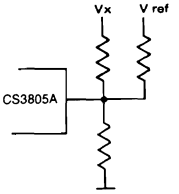
The input is a window comparator. A higher or lower voltage than the thresholds specified will shut down the power supply until voltage falls within the window again, at which point the CS-3805A goes into soft-start. If pin 15 is not used, it must be tied to V_{cc} or the 5V reference via a voltage divider, generating a bias voltage, which falls within the window. The voltage divider should carry approximately 1mA. The maximum input voltage on this pin is 6V.

Because one pin is available for this window comparator a two-resistor voltage divider will only satisfy the requirements of one voltage range of V_x, from V_{x1} to V_{x2}, where the expression given in Fig. 12a applies. If the voltage to be monitored, V_x, has a range satisfying the expression given in Fig. 12b then the corresponding circuit arrangement can be used. If the range of V_x is such that $(V_{x2} - V_{x1})/V_{x2}$ is less than .33 one can add a Zener diode as shown in Fig. 12c with a Zener voltage that will satisfy the corresponding expression given in this figure.



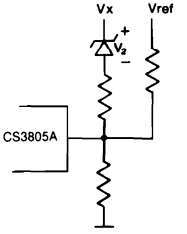
$\frac{V_{x2}-V_{x1}}{V_{x2}} = .33$

Figure 12a



$\frac{V_{x2}-V_{x1}}{V_{x2}} > .33$

Figure 12b



$\frac{V_{x2}-V_{x1}}{V_{x2}-V_z} > .33$

Figure 12c

Pin 16 (OL) - Overload Input
A voltage exceeding the specified threshold on this pin will cause the CS-3805A to shut down and activate the overload restart delay function. This delay starts when the input voltage drops below this threshold. On time-out, soft-start begins. The maximum input voltage on this pin is 6V. If pin 16 is not used, it should be shorted to ground. No capacitor is required on pin 2 (ORLD), but a bias voltage between $V_{cc}/3$ and $V_{cc}/3$ + 5.7V is still needed. A convenient voltage is $V_{cc}/2$.

A TYPICAL APPLICATION CONFIGURATION
Figure 13 shows the CS-3805A as a resonant mode power supply. L_r and C_r form the series resonant tank. V_{cc} is generated locally for high efficiency, using a start-up circuit which is biased off by a auxiliary transformer winding voltage after V_{cc} stabilizes. T2 senses the current in the primary of T3 and provides the overload signal.

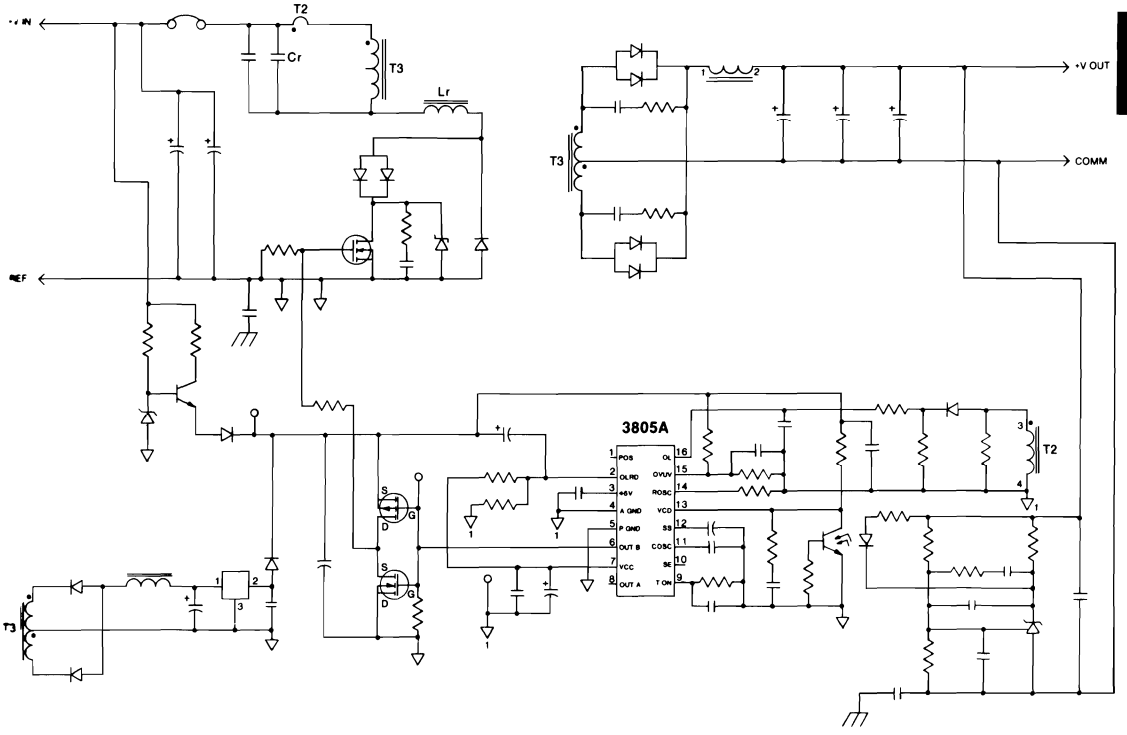


Fig. 13 Typical Application

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-3805AN	16L PDIP
CS-3805ADW	16L SO WIDE

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_Z	Reverse Breakdown Voltage	T_A = 25°C, I_R = 1mA		2.495	2.500	2.505	V
$\frac{\Delta V_Z}{\Delta 1_R}$	Reverse Breakdown Change with Current	400μA≤IR≤10mA	 •		2.6 3	10 12	mV mV
r_Z	Reverse Dynamic Impedance	I_R = 1mA	 •		0.2 0.4	1.0 1.4	Ω Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability Average Temperature Coefficient	0°C≤T_A≤70°C (Note 1) 0°C≤T_A≤70°C (Note 1)			1.8 15	4 25	mV ppm/°C
$\frac{\Delta V_Z}{\Delta Timc}$	Long Term Stability	T_A = 25°C±0.1°C, I_R = 1mA			20		ppm/kHr

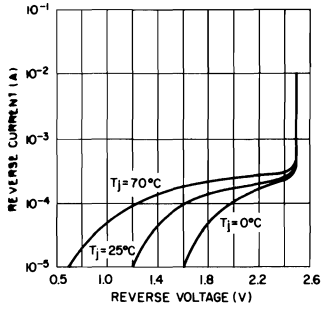
The • denotes the specifications which apply over full operating temperature range.

Note 1: These parameters although guaranteed by design, are not tested during production. Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

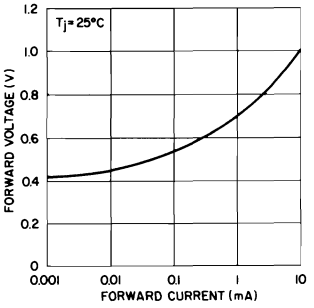
4

TYPICAL PERFORMANCE CHARACTERISTICS

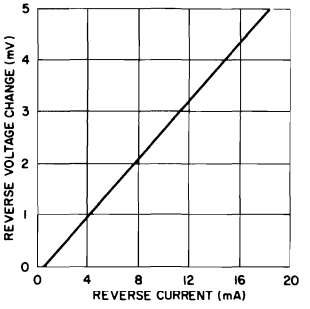
REVERSE CHARACTERISTICS



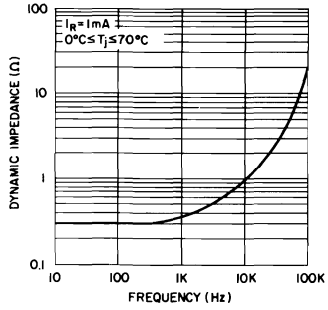
FORWARD CHARACTERISTICS



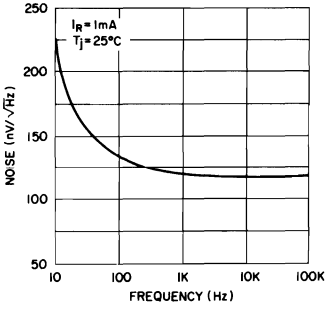
REVERSE VOLTAGE CHANGE



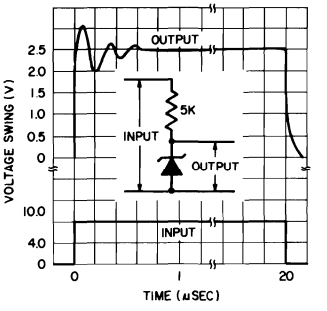
DYNAMIC INPEDANCE



ZENER NOISE VOLTAGE



RESPONSE TIME



ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_Z	Reverse Breakdown Voltage	T_A = 25°C, I_R = 1mA		2.495	2.500	2.505	V
$\frac{\Delta V_Z}{\Delta 1_R}$	Reverse Breakdown Change with Current	400μA≤IR≤10mA	 ●		2.6 3	10 12	mV mV
r_Z	Reverse Dynamic Impedance	I_R = 1mA	 ●		0.2 0.4	1.0 1.4	Ω Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability Average Temperature Coefficient	0°C≤T_A≤70°C (Note 1) 0°C≤T_A≤70°C (Note 1)			1.8 15	4 25	mV ppm/°C
$\frac{\Delta V_Z}{\Delta Timc}$	Long Term Stability	T_A = 25°C±0.1°C, I_R = 1mA			20		ppm/kHr

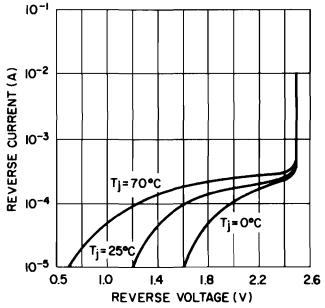
The ● denotes the specifications which apply over full operating temperature range.

Note 1: These parameters although guaranteed by design, are not tested during production. Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

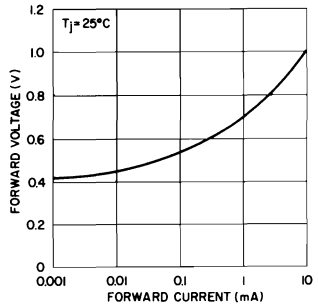
4

TYPICAL PERFORMANCE CHARACTERISTICS

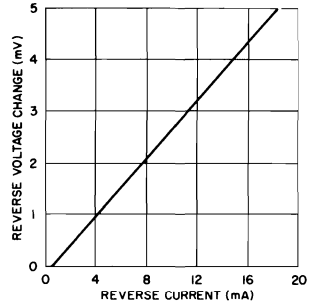
REVERSE CHARACTERISTICS



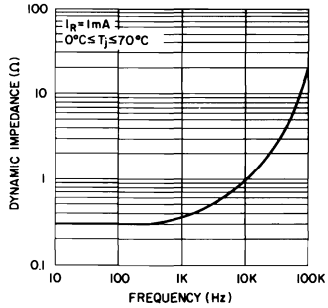
FORWARD CHARACTERISTICS



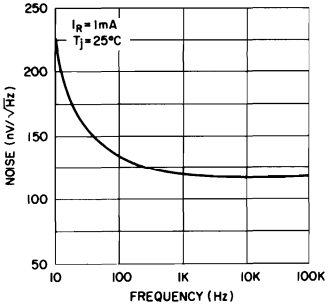
REVERSE VOLTAGE CHANGE



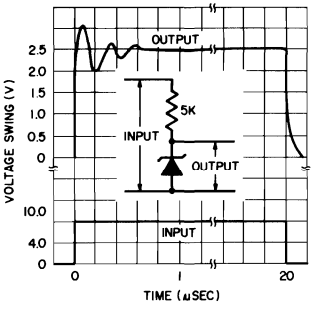
DYNAMIC INPEDANCE



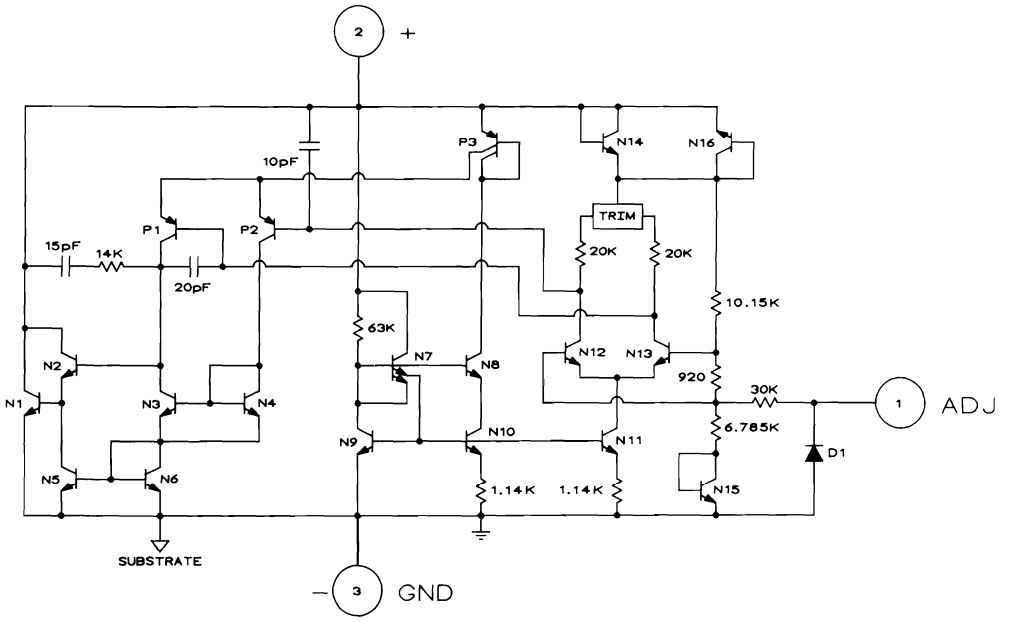
ZENER NOISE VOLTAGE



RESPONSE TIME

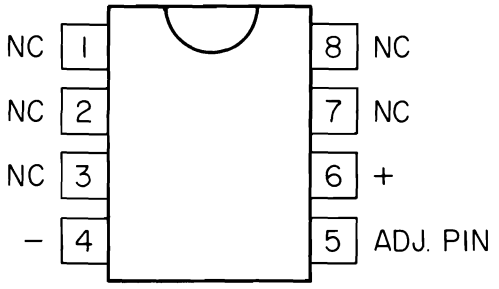


SCHEMATIC DIAGRAM



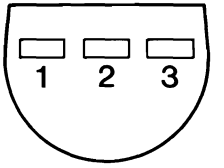
PIN CONNECTIONS

SO-8



TO-92

BOTTOM VIEW



1. **ADJ**
2. +
3. –

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE
CS-1009D	SO-8
CS-1009	TO-92

CSC™ CHERRY SEMICONDUCTOR

CS-2706
CS-3706

DUAL OUTPUT DRIVER

DESCRIPTION

The CS-2706/CS-3706 series of integrated circuits provide an interface between low-level TTL inputs and high-power switching devices such as power MOSFETs. A typical application is single-ended PWM control to push-pull power control conversion.

The primary function of these devices is to convert a bipolar single-ended low current digital input to a pair of totem pole outputs which can source or sink up to 1.5A each. An internal flip-flop, driven by double-pulse suppression logic, can be enabled to provide single-ended to push-pull conversion. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control and thermal shutdown.

FEATURES:

- Dual 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiesent Current
- 5V to 40V Operation
- Thermal Shutdown Protection

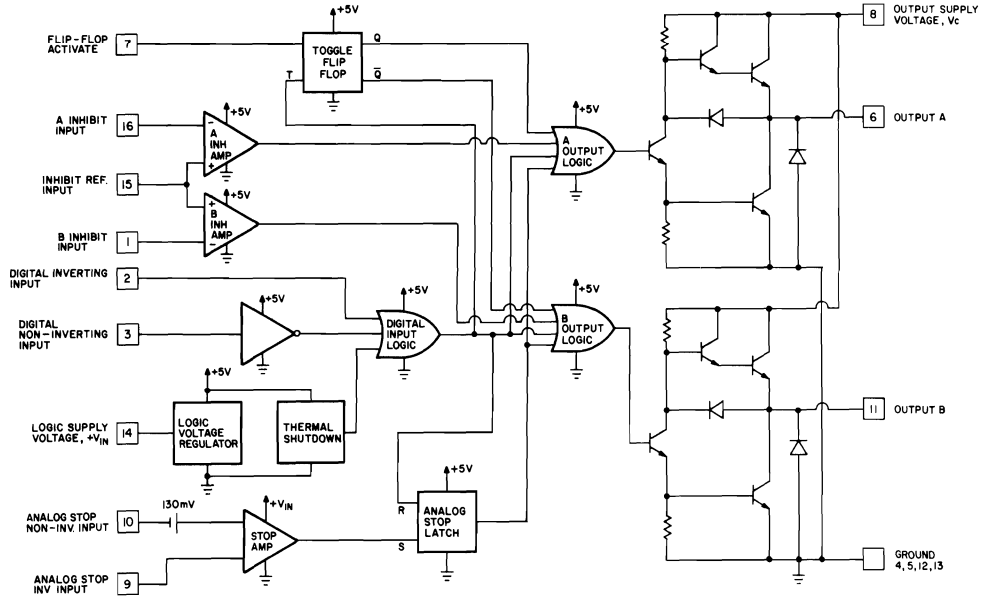
TRUTH TABLE

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.

$\overline{\text{OUT}}$ = INV or $\overline{\text{N.I.}}$

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

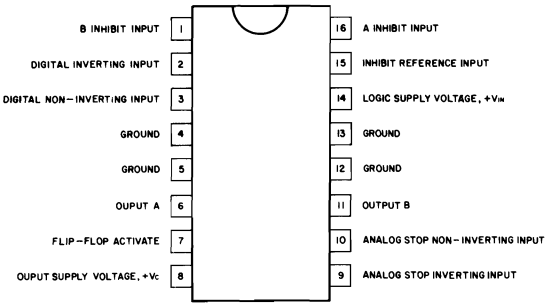
	N-PACKAGE (Plastic)	UNITS
Logic Supply Voltage (Vin, Pin 14)	40.0	V
Output Supply Voltage (Vc, Pin 8)	40.0	V
Output Current (each output, source, or sink) (pins 6 & 11)		
Steady State	±500	mA
Peak Transient for Less Than 100us	±1.5	A
capacitive discharge energy	20.0	uJ
Digital Inputs (pins 2 & 3)	5.5	V
Analog Inputs (pins 9 & 10)	Vin	V
Inhibit Inputs (pins 1, 15, & 16)	5.5	V
Power Dissipation at TA=25°C	2.0	W
Derate Above 50°C	20.0	mW/°C
Power Dissipation at T (leads and case)=25°C	5.0	W
Derate for Ground Lead Temperature Above 25°C	40.0	mW/°C
Derate for Case Temperature above 25°C	—	mW/°C

Operating Temperature Range	
CS-2706	-25 to 85°C
CS-3706	0 to 70°C
Storage Temperature Range	-65 to 150°C
Lead Temperature (soldering, 10 sec)	300 °C

NOTES: All voltages are with respect to the four ground pins which must be connected together.

All currents are positive into, negative out of the specified terminal.

PIN CONNECTIONS



NOTE: ALL FOUR GROUND PINS MUST BE CONNECTED TO A COMMON GROUND

ELECTRICAL CHARACTERISTICS These specifications apply over the operating temperature range of the IC. (V_{IN} = V_C = 20V, V_4 = V_5 = V_{12} = V_{13} = 0V unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V, V_C = 20V, V_2 = 0V, Unused pins = open.		8	12	mA
V_C Supply Current	V_{IN} = 20V, V_C = 40V, Outputs low		3	5	mA
V_C Leakage Current	V_{IN} = 0V, V_C = 40V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Digital Input Current	V_I = 0V		-0.6	-1.0	mA
Digital Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_O = -50mA			2.0	V
Output High Sat., V_C-V_O	I_O = -500mA			2.5	V
Output Low Sat., V_O	I_O = 50mA			0.4	V
Output Low Sat., V_O	I_O = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
Inhibit Threshold	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0V		-10	-20	μA
Analog Threshold	V_{CM} = 0V to 15V	100	130	150	mV
Analog input bias current	V_I = 0V, V_{CM} = 15V		-10	-20	μA
Thermal Shutdown	Turn on (TA)		155		°C
Thermal Shutdown	Turn off (TA)		125		°C

TYPICAL SWITCHING CHARACTERISTICS (V_{IN} = V_C = 20V, T_A = 25°C. Delays measured 50% in to 50% out.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N.I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_c Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V Inhibit = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (-) Input = 0 to 0.5V	180			ns

4

CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast. high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec. must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs—the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} - 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply, however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C. When combined with a CS-384X PWM, the Driver Bias switch can be used to supply V_{IN} to the CS-3706. V_{IN} switching should be fast as undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

PACKAGE/TEMPERATURE RANGE OPTIONS

Part Number	Package	Temperature Range	Power @ 25°C
CS-3706N	16 Pin Plastic Batwing DIP	0°C to 70°C	2W
CS-2706N	16 Pin Plastic Batwing DIP	-25°C to +85°C	2W

CHERRY SEMICONDUCTOR

CS-293D

PUSH-PULL FOUR CHANNEL 600mA DRIVER

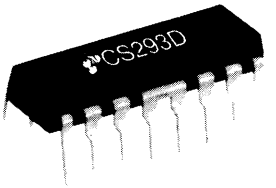
DESCRIPTION

The CS-293D is a quad push-pull driver integrated circuit capable of delivering output current to 600mA per channel. Each channel is controlled by a TTL-compatible logic input. Each full-bridge driver is equipped with an enable input which turns off all four transistors. A separate logic supply input is provided so that it may operate from a lower voltage to reduce power dissipation. The CS-293D also includes output clamping diodes for interfacing with inductive loads.

The CS-293D is available in a 16 lead plastic power DIP.

ABSOLUTE MAXIMUM RATINGS

V_c	Collector Supply Voltage	36V
V_{ss}	Logic Voltage	36V
I_{out}	Peak Output Current (non-repetitive)	1.2A
P_{tot}	Total Power Dissipation at $T_{ground-pins}$=80°C	5W
T_{stg}, T_j	Storage and Junction Temperature	-40 to +150°C

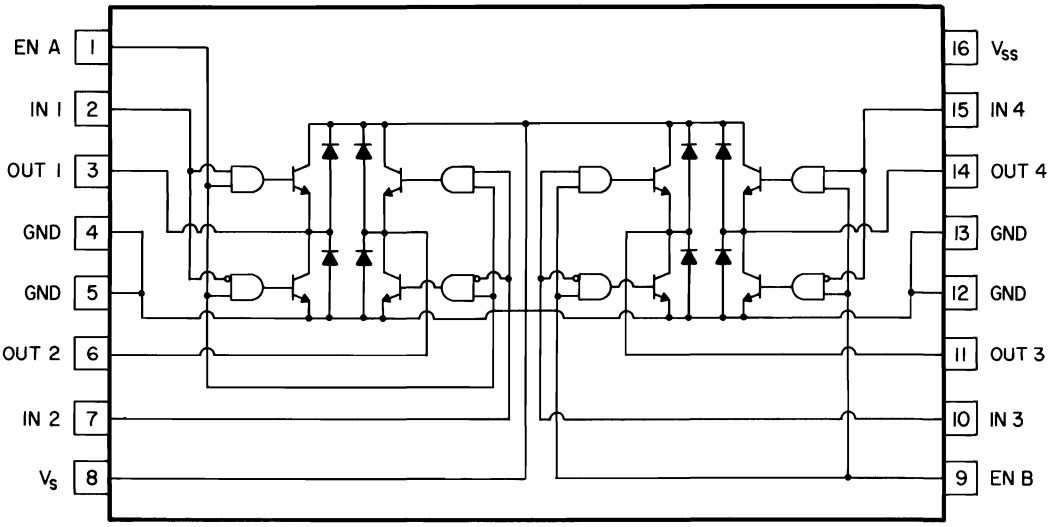


FEATURES:

- Output current 600mA per channel
- Peak output current 1.2A per channel
- Inhibit capability
- High noise immunity
- Separate logic supply
- Over-temperature protection

5

BLOCK DIAGRAM



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS (For each channel, V_s=24V, V_{ss}=5V, T_{amb}=25°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_s	Supply voltage		V_{ss}		36	V
V_{ss}	Logic supply voltage		4.5		36	
I_s	Total quiescent supply current	V_i=L I_o=0 V_{en}=H		12	32	mA
		V_i=H I_o=0 V_{en}=H		75	95	
		V_{en}=L			4	
I_{ss}	Total quiescent logic supply current			3.5	7	mA
V_{il}	Input low voltage		-0.3		0.8	V
V_{ih}	Input high voltage		2.0		V_s	V
I_{il}	Low voltage input current	$V_i \leq V_{il}$ max		-50	-100	uA
I_{ih}	High voltage input current	$V_i \geq V_{ih}$ min			10	uA
V_{enl}	Enable low voltage		-0.3		0.8	V
V_{enh}	Enable high voltage		2.0		V_s	V
I_{enl}	Low voltage enable current			-50	-100	uA
I_{enh}	High voltage enable current				10	uA
$VCE_{sat}H$	Source output saturation voltage	I_O=Imax cont.		1.4	1.8	V
$VCE_{sat}L$	Sink output saturation voltage	I_O=Imax cont.		1.2	1.8	V
VF	Diode forward voltage	ID=.6A		1.6	1.8	V

SWITCHING CHARACTERISTICS (see diagram) V_s=24V, V_{ss}=5V, f_c=30KHz, T_A=25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ton	Sink Current turn-on Delay		2000		ns
tr	Sink Current Rise Time		200		ns
toff	Sink Current Turn-off Delay		600		ns
tf	Sink Current Fall Time		200		ns
ton	Source Current Turn-on Delay		2000		ns
tr	Source Current Rise Time		600		ns
toff	Source Current Turn-off Delay		700		ns
tf	Source Current Fall Time		400		ns
td1	Sink to Source Deadtime	0	1000		ns
td2	Source to Sink Deadtime	0	1000		ns

THERMAL DATA

RO_{JC} ..... MAX 14° C/W
RO_{JA} ..... MAX 80° C/W

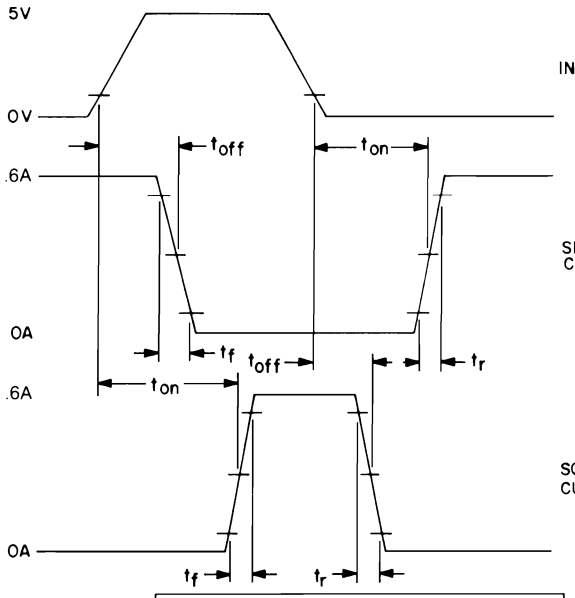
SWITCHING DIAGRAM

TRUTH TABLE

INPUT	ENABLE*	OUTPUT
H	H	H
L	H	L
H	L	Z
L	L	Z

* RELATIVE TO THE CONSIDERED CHANNEL

Z = HIGH IMPEDANCE

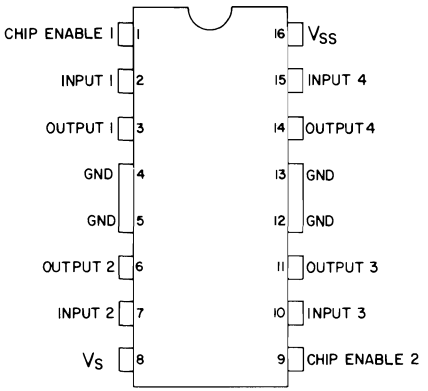


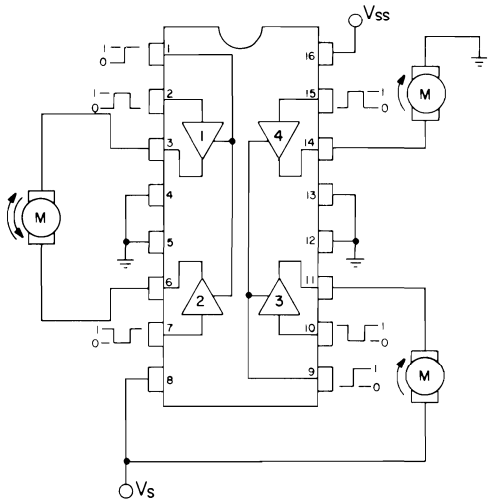
$t_{d1} = (t_{on} - t_r/2)_{source} - (t_{off} + t_f/2)_{sink}$

$t_{d2} = (t_{on} - t_r/2)_{sink} - (t_{off} + t_f/2)_{source}$

5

CS-293D CONNECTION DIAGRAM AND TYPICAL APPLICATION





MOUNTING INSTRUCTIONS

The $R\theta_{JA}$ of the CS293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

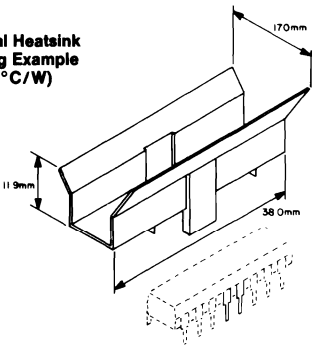
The diagram of Figure B shows the maximum package power P_{tot} and the θ_{JA} as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (see figure C).

In addition, it is possible to use an external heatsink (see figure A).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. A - External Heatsink Mounting Example (θ_{JA}=25°C/W)



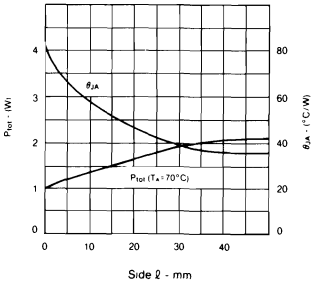


Fig. B - Maximum Power Dissipation and Junction to Ambient Thermal Resistance vs Side "ℓ"

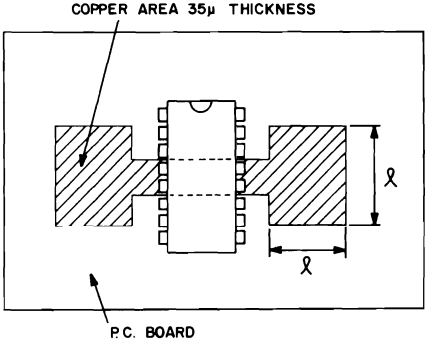


Fig. C - Example of P.C. Board Copper Area which is used as Heatsink

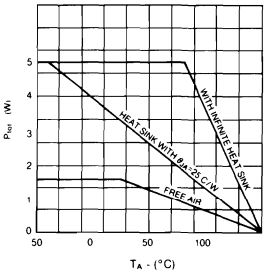


Fig. D - Maximum Allowable Power Dissapation vs Ambient Temperature

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-293D	16 Lead Plastic Power DIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-298

DUAL FULL-BRIDGE DRIVER

DESCRIPTION

The CS-298 is a power integrated circuit capable of driving resistive and inductive loads such as relays, solenoids, DC and stepping motors. This device is a quad push-pull driver with the ability to deliver up to 2A of continuous current per channel.

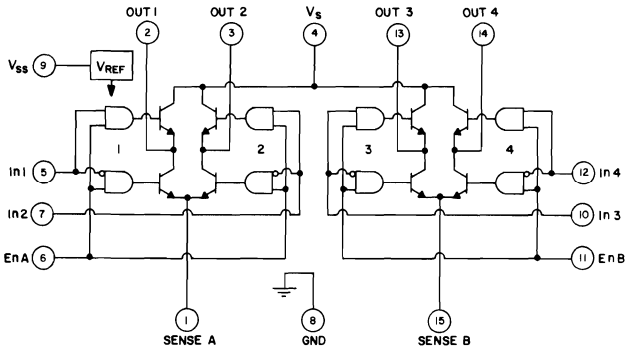
Each pair of drivers is equipped with an inhibit input which disables the associated drive stage independent of input signals. This is convenient for powering the device down or utilizing it in the chop mode. The logic inputs to the CS-298 have high input thresholds and hysteresis to provide trouble free operation in noisy environments normally associated with motors and inductive loads. The input currents and thresholds enable the device to be driven by TTL and CMOS systems without buffering or level shifting.

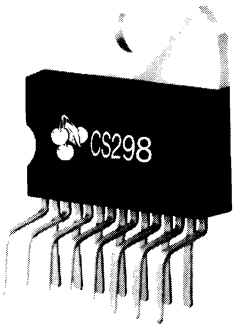
The emitters of the lower transistors of each bridge are connected together and the corresponding pin can be connected to a sense resistor which, when used with an appropriate external circuit, can detect load faults or control load currents when the device is in switch mode operation.

This device also features separate logic supply and load supply inputs to reduce total IC power consumption, thus making the CS-298 ideal for systems which require low-standby current.

The CS-298 is packaged in a 15-lead Multiwatt package which handles up to 2A per channel at voltages of 46 volts.

BLOCK DIAGRAM

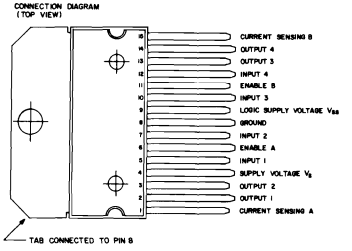




FEATURES:

- Operating Supply Voltage up to 46V.
- Total Saturation Voltage 3.4V max at 1A.
- Overtemperature Protection.
- Operates in Switched and Linear Regulation Modes.
- 25W Power-Tab Package for Low Installed Cost.
- Individual Logic Inputs for Each Driver.
- Channel-Enable Logic Inputs for Driver Pairs.

PIN CONNECTIONS



5

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNITS
Power Supply	V_S	50	V
Logic Supply Voltage	V_{SS}	7	V
Input and Inhibit Voltage	V_i, $V_{inhibit}$	-0.3 to +7	V
Peak Output Current (each channel)	I_O		
Non-Repetitive (+=100μs)		3	A
Repetitive (80% on 20% off; ton=10ms)		2.5	A
DC Operation		2	A
Sensing Voltage	V_{sens}	-1 to +2.3	V
Total Power Dissipation (T_{case}=75°C)	P_{tot}	25	W
Storage and Junction Temperature	T_{stg}, T_J	-40° to +150°	C

ELECTRICAL CHARACTERISTICS (for each channel, V_s=42V, V_{ss}=5V, T_j=25°C)

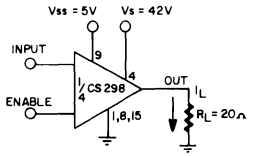
PARAMETER	SYMBOL	PIN #'S	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_S	4	Operative Condition	V_{IH}+2.5		46	V
Logic Supply Voltage	V_{SS}	9		4.5		7	V
Quiescent Supply Current	I_S	4	$V_{inh.}$=H V_i=L		3	7	mA
			I_L=0 V_i=H		15	20	
			$V_{inh.}$=L			1	
Quiescent Current from V_{SS}	I_{SS}	9	V_{inh}=H V_i=L		5	10	mA
			I_L=0 V_i=H		1.5	3	
			$V_{inh.}$=L		1	1.5	
Input Low Voltage	V_{iL}	5, 7, 10, 12		-0.3		1.5	V
Input High Voltage	V_{iH}	5, 7, 10, 12		2.3		V_{ss}	
Low Voltage Input Current	I_{iL}	5, 7, 10, 12	V_i=L			-10	μA
High Voltage Input Current	I_{iH}	5, 7, 10, 12	V_i=H		30	100	
Inhibit Low Voltage	$V_{inh\ L}$	6, 11		-0.3		1.5	V
Inhibit High Voltage	$V_{inh\ H}$	6, 11		2.3		V_{ss}	
Low Voltage Inhibit Current	$I_{inh\ L}$	6, 11	$V_{inh.}$=L			-10	μA
High Voltage Inhibit Current	$I_{inh\ H}$	6, 11	$V_{inh.}$=H$\leq V_{SS}$ -0.6V		30	100	
Source Saturation Voltage	$V_{CE\ sat(H)}$		I_L=1A		1.2	1.8	V
			I_L=2A		1.8	2.8	
Sink Saturation Voltage	$V_{CE\ sat\ (L)}$		I_L=1A		1.2	1.8	V
			I_L=2A		1.7	2.6	
Total Drop	$V_{CE\ sat}$		I_L=1A			3.4	V
			I_L=2A			5.2	
Sensing Voltage	V_{SENS}	1, 15		-1 (1)		2	V
Source Current Turn-Off Delay	T_1		0.5V_i to 0.9 I_L (2)		1.7		μs
Source Current Fall Time	T_2		0.9 I_L to 0.1 I_L (2)		0.2		μs
Source Current Turn-On Delay	T_3		0.5 V_i to 0.1 I_L (2)		2.5		μs
Source Current Rise Time	T_4		0.1 I_L to 0.9 I_L (2)		0.35		μs
Sink Current Turn-off Delay	T_5		0.5 V_i to 0.9 I_L (3)		0.7		μs
Sink Current Fall Time	T_6		0.9 I_L to 0.1 I_L (3)		0.2		μs
Sink Current Turn-on Delay	T_7		0.5 V_i to 0.1 I_L (3)		1.5		μs
Sink Current Rise Time	T_8		0.1 I_L to 0.9 I_L (3)		0.2		μs
Commutation Frequency	f_c		I_L=2A		25	40	KHz

1) Sensing voltage can be -1V for t$\leq$50μS; in steady state V_{sens} min$\geq$ -0.5V.
2) See figure 1a.
3) See figure 2a.

THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j-case}$ .....3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j-amb}$.....35°C/W max.

FIGURE 1 SWITCHING TIMES TEST CIRCUITS



NOTE: FOR INPUT CHOPPER, SET EN = H

FIGURE 1A SOURCE CURRENT DELAY TIMES VS. INPUT OR ENABLE CHOPPER.

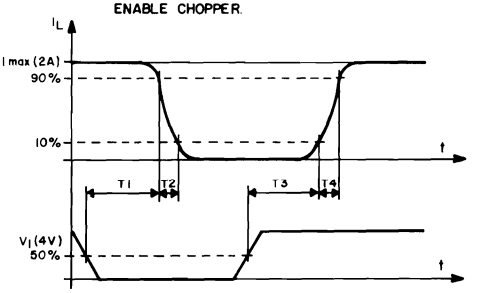
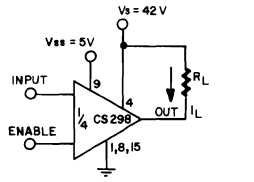
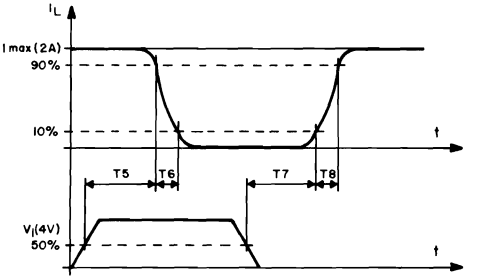


FIGURE 2. SWITCHING TIMES TEST CIRCUITS.



NOTE: FOR INPUT CHOPPER, SET EN = H

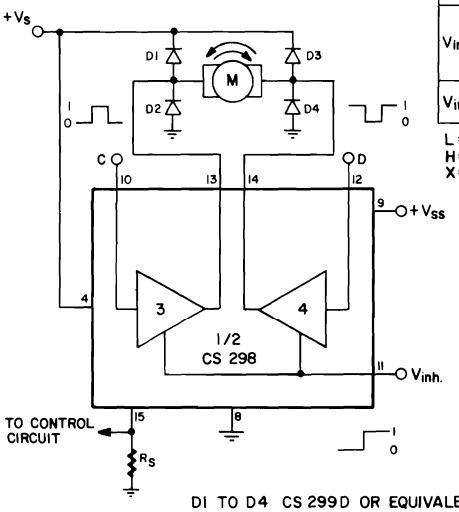
FIGURE 2A. SINK CURRENT DELAY TIMES VS. INPUT OR ENABLE CHOPPER.



5

TYPICAL APPLICATION

FIGURE 3. BI-DIRECTIONAL DC MOTOR CONTROL.



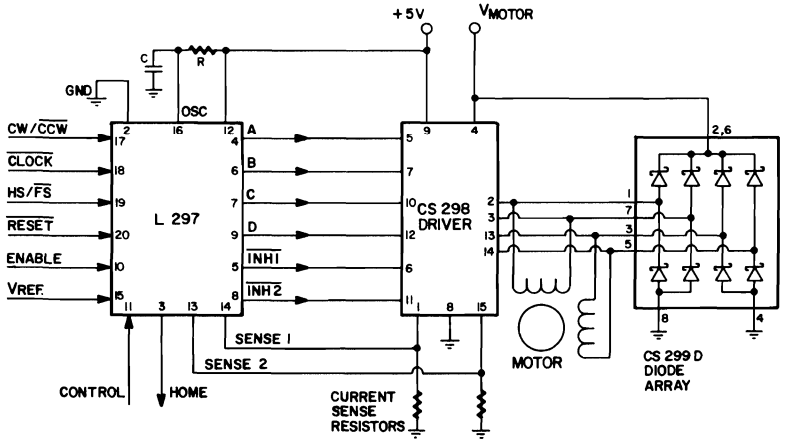
	INPUTS	FUNCTION
$V_{inh.} = H$	C = H; D = L	TURN RIGHT
	C = L; D = H	TURN LEFT
	C = D	FAST MOTOR STOP
$V_{inh.} = L$	C = X; D = C	FREE RUNNING MOTOR STOP

L = LOW
H = HIGH
X = DON'T CARE

D1 TO D4 CS 299D OR EQUIVALENT

TYPICAL APPLICATION

FIGURE 4.- TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT
THIS CIRCUIT DRIVES BIPOLAR STEPPER MOTOR WITH WINDING CURRENTS UP TO 2A.



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-298	15 Lead Multiwatt®

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-299D

DUAL SCHOTTKY DIODE BRIDGE

DESCRIPTION

The CS-299D is an eight-diode array designed for flyback voltage clamping of inductive loads, where high peak current and low duty-cycle conditions exist. The dual-bridge configuration makes the CS-299D particularly well suited for bipolar stepper motor driver applications.

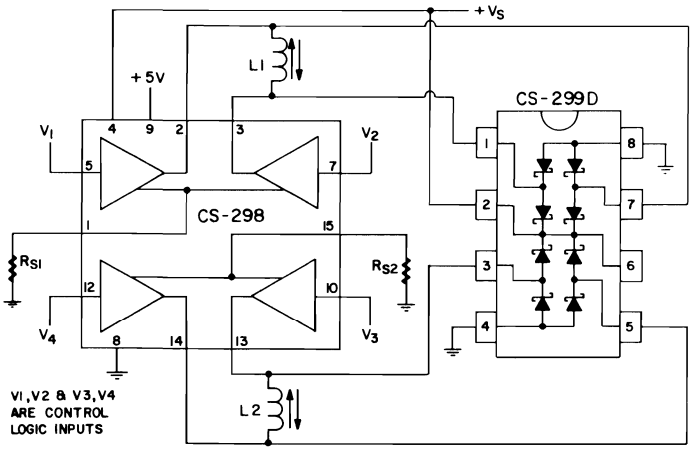
CSC Schottky diode technology provides highly efficient operation due to low forward voltage drop, and fast reverse recovery time.

The CS-299D is available in hermetic CERDIP, and in copper lead-frame plastic MINI-DIP. The CS-299D (I) in CERDIP is for the industrial temperature range of -25 to +85°C, while the CS-299D (C) in plastic is for the commercial temperature range of 0 to +70°C.

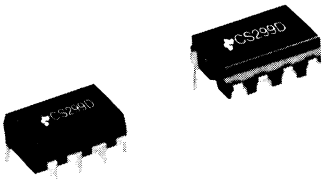
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
CS-299D(I) 2A
CS-299D(C) 3A
Power Dissipation at T_A = 70°C 1W
Derate 12.5mW/°C above 70°C
Storage Temperature Range ..... -65°C to +150°C

BLOCK DIAGRAM



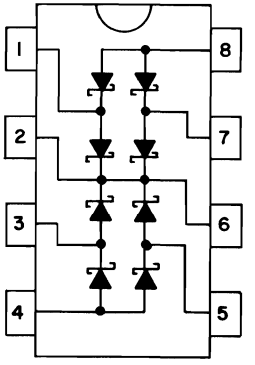
TYPICAL APPLICATION: CS-299D WITH CS-298 STEPPER MOTOR DRIVER



FEATURES:

- 8-Diode array
- High efficiency
- 3A peak current
- Fast recovery time
- Low forward voltage
- Dual bridge configuration for ease of application
- Plastic or CERDIP packages available

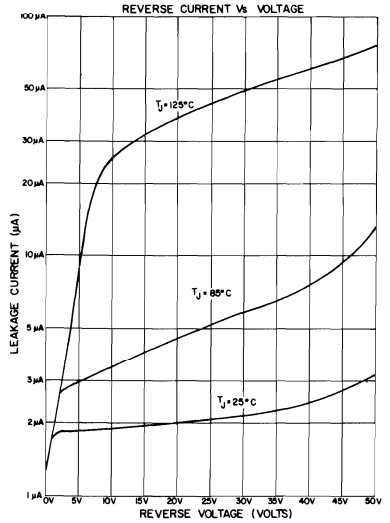
PIN CONNECTIONS (TOP VIEW)

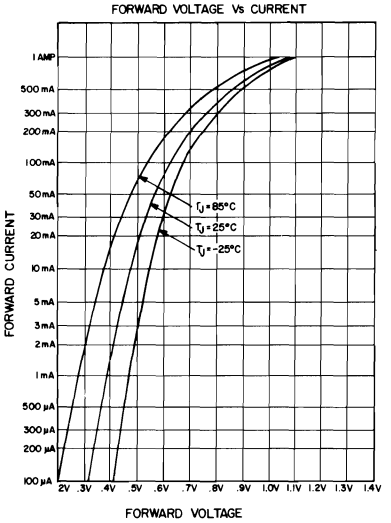


5

ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = 25°C except as noted.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA	0.4	0.5	0.7	V
	I_F = 1A	0.8	1.0	1.3	
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = 100°C		0.1	1.0	
Reverse Recovery	.5A Forward to .5A Reverse		15		nSec
Forward Recovery	1A Forward to 1.1V Recovery		30		nSec
Junction Capacitance	V_R = 5V		70		pF





ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-299D	8 Lead PDIP

CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-365

3A POWER OPERATIONAL AMPLIFIER

DESCRIPTION

The CS-365 is a monolithic integrated circuit available in a TO-220 package. It is intended for use as a power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capabilities provide superior performance wherever an operational amplifier/power booster combination is required.

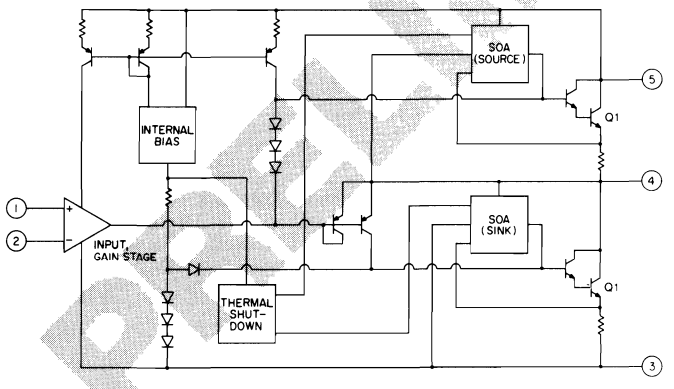
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18	V
Upper power transistor V_{CE}	36	V
Lower power transistor V_{CE}	36	V
Input voltage	V_s	
Differential input voltage	±15	V
Peak output current	3.5	A
Power dissipation at T_{case} = 90°C	20	W
Storage and junction temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$ Thermal resistance junction-case	max	3	°C/W

BLOCK DIAGRAM

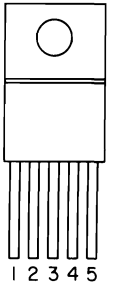


FEATURES:

- Output current up to 3A
- Large common-mode and differential mode ranges
- SOA protection
- Thermal protection
- ±18V supply

PIN CONNECTIONS

Tab (Pin 3)



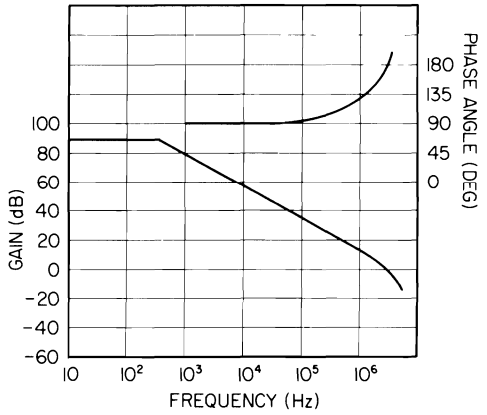
1. NON INVERTING INPUT
2. INVERTING INPUT
3. $-V_S$
4. OUTPUT
5. $+V_S$

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

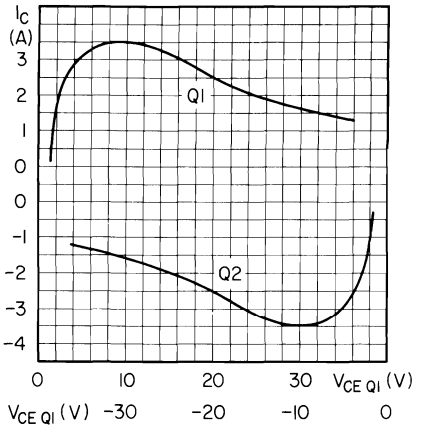
ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_j = ± 25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage		±6		±18	V
Quiescent drain current	V_s = ± 18V		40	60	mA
Input bias current			0.2	1	μA
Input offset voltage			±2	±10	mV
Input offset current			±20	±200	nA
Slew-Rate	G_v = 10		8		V/μs
	G_v = 1		6		
Output voltage swing	f = 1kHz I_p = 0.3A		27		V_{pp}
	I_p = 3A		24		
	f = 10kHz I_p = 0.3A		27		V_{pp}
	I_p = 3A		23		
Input resistance (pin 1)	f = 1kHz	100	500		KΩ
Voltage gain (open loop)			80		dB
Input noise voltage	B = 10 to 10,000 Hz		2		μV
Input noise current			100		pA
Common mode rejection	$R_g \leq$ 10 KΩ G_v = 30 dB		70		dB
Supply voltage rejection	R_g = 22 kΩ G_v = 10		60		dB
	V_{ripple} = 0.5 V_{rms}				
	f_{ripple} = 100 Hz G_v = 100		40		dB
Efficiency	f = 1 kHz I_p = 1.6A; P_o = 5W		70		%
	R_L = 4Ω I_p = 3A; P_o = 18W		60		%
Thermal shut-down case temperature	P_{tot} = 12W		110		°C
	P_{tot} = 6W		130		

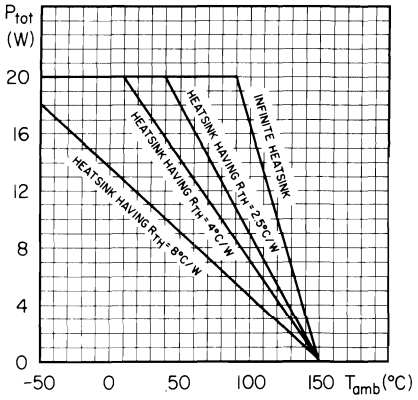
Open loop frequency response



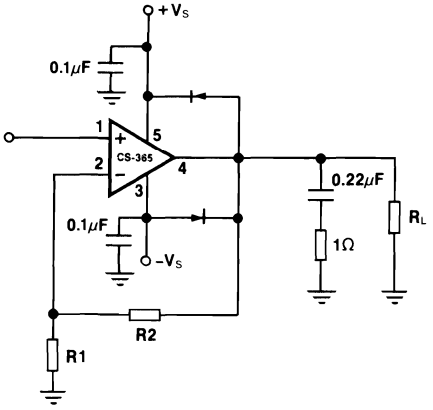
Maximum output current vs. voltage (V_{CE}) across each output transistor



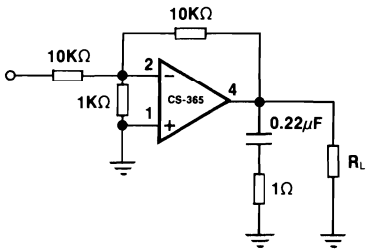
Maximum allowable power dissipation vs. ambient temperature



Application circuit (G_V>10)



Unity gain configuration



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-365	TO-220

CHERRY SEMICONDUCTOR

CS-2907
CS-2917

F TO V CONVERTER
LOW COST MULTI-FUNCTION ICs

DESCRIPTION

The CS-2907/2917 Series is designed for use in frequency-to-voltage conversion systems and is especially suitable for tachometer and motor-speed-control applications. The 2907 consists of a regenerative input comparator, a frequency doubling charge pump and a general purpose, differential op-amp output. The 2917 has the additional built-in feature of an internal shunt voltage regulator. The input signal, which can be single-ended, or differential, is applied to the regenerative comparator input; 30mV hysteresis provides noise rejection.

The frequency-doubling charge pump is triggered by the comparator output, converting the input-frequency information into a d.c. output voltage at Pin 3. The output op-amp is unity-gain compensated and can serve as an output-voltage follower or as an active filter for additional ripple reduction. 50mA current capability allows the output stage to drive a variety of loads either from emitter, or collector.

The output swings to ground for zero frequency input.

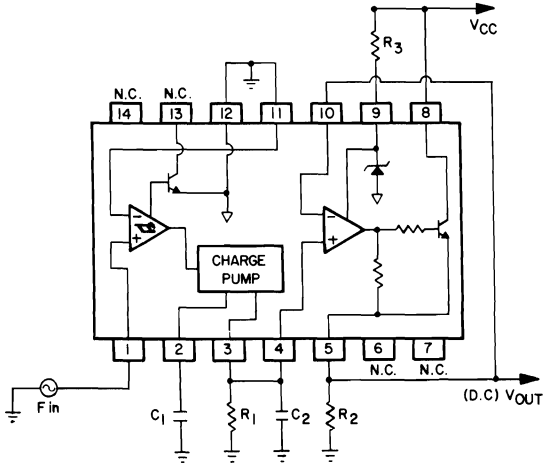
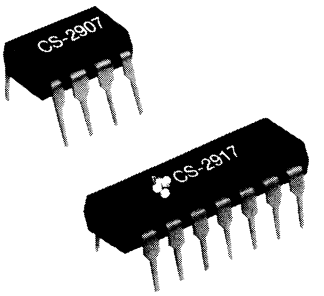


Fig.1

APPLICATIONS

A timing capacitor C1, an output resistor R1, and an output filter capacitor C2, are required as shown in Fig. 1. On each transition of the input comparator, C2 is linearly charged or discharged



FEATURES

- ± 0.3% Linearity, Typical
- Buffered High-Level Frequency Output
- Single-ended or Differential Inputs
- Voltage Follower or Active Filter Output Capability
- Output Swings to Ground for Zero Frequency Input

APPLICATIONS

- Motor Speed Control
- Cruise Control
- Speedometer/Tachometer
- Over/Under Speed Control
- Magnetic and Optical Sensor Interfacing
- Zero Crossing Detector
- Frequency Discrimination

between voltage limits Vh and Vl. The difference, Vh - Vl, equals Vcc/2. During one half cycle of input frequency, the change in charge on C1 is: C1 Vcc/2. The average charge-pump current charging C1 during one half cycle of input frequency = C1VccFin where Fin = input frequency. This charge pump current, Ic, is accurately mirrored into R1 to generate a DC voltage at pin 3 such that Vpin3 = IcR1 = K R1C1 Vcc Fin where K is a circuit constant typically equal to one. Averaging, or filtering is accomplished with C2 and both output ripple voltage and response time are dependent on the value of C2. Peak to peak ripple voltage, Vr = (Vcc/2)(C1/C2)(1-Fin/Fmax) where Fmax = I2/(C1Vcc) and I2 is the current in C2.

For the 2917 series on-board shunt-regulator an external resistor R3 is required for operation from the input supply voltage.

The value of R1 does not therefore affect ripple; however if it is too large by comparison with the output impedance seen at pin3, linearity will be adversely affected. Since the current at pin3, I3, is internally set, R1 must be chosen such that Vpin3 max. = I3R1.

MOTOR SPEED CONTROL APPLICATION

Cherry's CS-2917 F-to-V converter Integrated Circuit, with built-in operational amplifier, regulator, and output transistor is ideal for tachometer feedback motor speed control applications. Two typical application circuits are shown in Figure 2. Figure 2A employs the CS-2907-N14 operating from the Vcc line Figure 2B offers an alternative approach using the CS-2917-N8 operating from the Vcc line and using the internal regulator. In both circuits, the tachometer feedback-signal is applied to the comparator input, and the F-to-V conversion gain is set by R_1C_1. The general purpose op amp is used both as a summing node for the speed reference input (from potentiometer P_1), and as a frequency compensated integrator which provides zero steady state speed error under varying load conditions. Capacitors C_2 and C_3 provide the integrating function at low frequency while R_2 and C_2 provide the frequency compensation which insures loop stability, In Figure 2A, the on-chip driver transistor drives a discrete power transistor which in turn drives the motor. In Figure 2B, the on-chip driver transistor is used as an inverting gain stage to close the loop around the of amp, and the provide drive voltage for the discrete NPN darlington transistor which drives the motor.

Both of these approaches provide accurate regulation of motor speed under conditions of varying motor load, Vcc and ambient temperature.

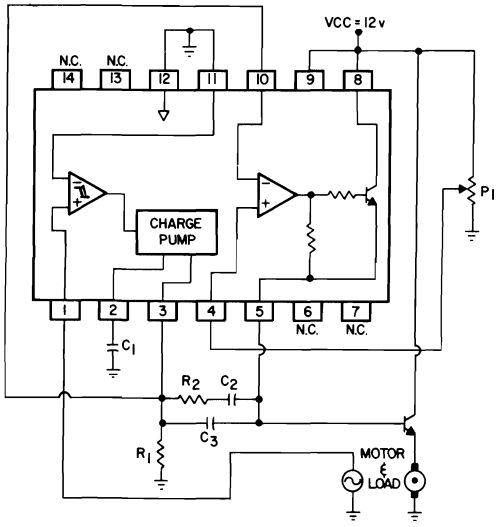


Fig. 2A

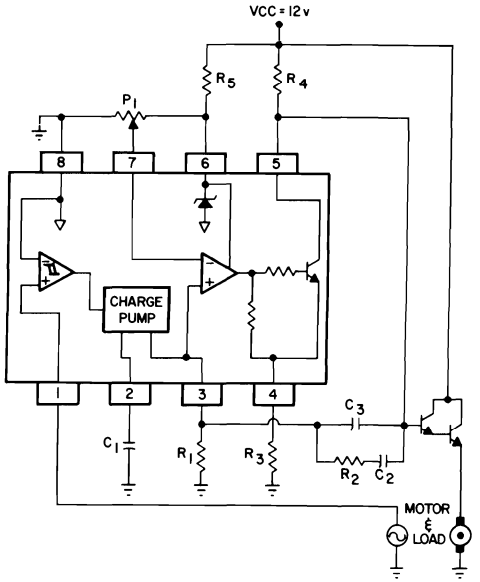


Fig. 2B

DESIGN EXAMPLE

Figure 3 is the circuit of Figure 2B re-drawn in a block diagram form which lends itself to visualization and analysis of the regulator loop. (Figure 2A can be analyzed in the same manner.) Potentiometer P1 provides the loop reference input. The op amp integrator, the power darlington and the motor provide the forward gain components K_1, K_2 and K_3. The tachometer and F-to-V converter provide the gain components K_4 and K_o in the feedback path. We will now derive the transfer functions for all components of the loop, write the expression for loop gain, and compute component values to insure loop stability.

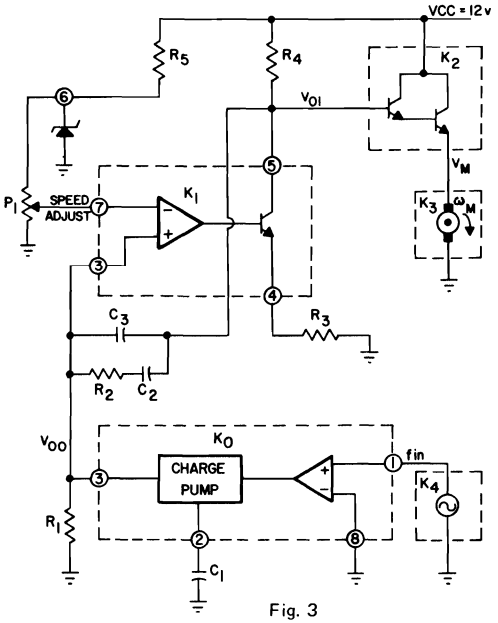


Fig. 3

A. K_o is the transfer function for the F-to-V converter.

1. $K_o = \frac{V_{oo}}{f_{in}} = K V_R R_1 C_1$, $K = 1.0$, $V_R = 7.6$ Volts

B. K_1 is the transfer function for the integrator.

2. $K_1 = \left|\frac{V_{o1}}{V_{oo}}\right| = \frac{1 + j\omega R_2 C_2}{J\omega R_1 (C_2 + C_3)\left[1 + \frac{j\omega C_2 C_3 R_2}{C_2 + C_3}\right]}$

This transfer function has the following poles and zeros:

Zero at: $\omega 1 = \frac{1}{R_2 C_2}$

Pole at: $\omega = 0$ (an integrator)

Pole at: $\omega 2 = \frac{C_2 + C_3}{R_2 C_2 C_3}$

C. K_2 is the transfer function of the power darlington transistor. Assume it equals 0.9 over the frequency range of interest.

3. $K_2 = \frac{V_m}{V_{o1}} = 0.9$

D. K_3 is the transfer function of the motor. (See Electro-craft Engineering Handbook, 4th edition, P9. 2-19, eq. 2.3.28.)

4. $K_3 = \frac{\omega_m}{V_m} = \frac{1/K_E}{(1+j\omega\mathcal{J}_m)(1+j\omega\mathcal{J}_e)}$

ω_m = Motor Rotational Speed (rad/sec)
V_m = Applied Motor Voltage
$\mathcal{J}_m = (R_A J_T / K_E K_T)$ = Mechanical Time Constant
$\mathcal{J}_e = (L_A / R_A)$ = Electrical Time Constant
K_T = Motor Torque Const. (oz · in/A)
K_E = Motor Back EMF Const. (V/rad/sec)
R_A = Motor Armature Resistance (ohms)
L_A = Motor Armature Inductance (henrys)
J_T = Total inertial Load on Motor (oz, · in · sec^2)

This design example describes an application using a small, permanent-magnet fractional-horsepower d.c. motor driving an inertial load. The following parameter values are taken from manufacturer's data for the motor and from laboratory measurements on the drive system.

$\omega_m = 314.2$ rad/sec (3000 rpm)

$K_T = 2.1$ oz. in/A $= 14.83 \times 10^{-3}$ N.M/A

$K_E = 14.83 \times 10^{-3}$ V/rad/sec

$R_A = 6.9\Omega$

$\mathcal{J}_e = 0.7$ msec

$\therefore L_A = 4.83$ mhy, and

$J_T = 9.39 \times 10^{-4}$ OZ·IN·SEC^2

$= 6.63 \times 10^{-6}$ Kg·m^2

5. $\mathcal{J}_m = \frac{R_A J_T}{K_E K_T} = 0.208$ sec

$\omega_B = \frac{1}{\mathcal{J}_m} = 4.8$ rad/sec

$f_B = 0.765$ HZ

$\omega_e = \frac{1}{\mathcal{J}_e} = 1429$ rad/sec

$f_e = 227$ HZ

$1/K_E = 67.4$

6. $K_3 = \frac{\omega_m}{V_m} = \frac{67.4}{(1 + j\frac{\omega}{4.8})(1 + j\frac{\omega}{1429})}$

Ignoring the electrical time constant (assumes that the loop crossover frequency is less than 1429 rad./sec.) we have:

7. $K_E = \frac{\omega_m}{V_m} = \frac{67.4}{(1 + j\frac{\omega}{4.8})}$

E. K_4 is the tachometer constant.

$\omega_m K_4 = f_{in}$

for $f_{in} = 400$ HZ, $\omega_m = 314.2$ rad/sec and

8. $K_4 = 1.273$ cyc/rad

The loop gain, A_L, equals.

9. $A_L = K_o K_1 K_2 K_3 K_4$ at $\omega = 1$ rad/sec, for $1 < W_B < W_1, < W_Z$

$$A_L(\omega = 1) = (7.6)(R_1C_1)\frac{(1)}{R_1(C_2 + C_3)}(0.9)(67.4)(1.273)$$

Arbitrarily selecting a loop gain of 50 (34db) at $\omega = 1$ rad/sec, we derive the following expression:

$$\frac{C_1}{C_2 + C_3} = \frac{50}{(7.6)(.9)(67.4)(1.273)} = 0.0852$$

10. $C_2 + C_3 = 11.74\,C_1$

Now, select R_1C_1 to set the loop reference voltage to about ½ of the on-chip zener reference voltage:

11. $K_4\,\omega_m \cdot K_o = V_{ref} \approx 7.6/2$

By selecting standard values for C_1 and R_1, $C_1 = 0.01$uF and $R_1 = 146K\Omega$, the reference voltage at the loop operating point is:

12. $V_{ref} = (314.2 \text{ rad/sec})(7.6)(1.0)(.01\text{uF})(146\text{k})(1.273) = 4.4$ volts

4.4 volts is well within the regulated supply tolerance and should present no adjustment problem in production.

Now, plot the bode diagram for the loop with only the integrator response and motor break frequency, $f_B = 0.765$HZ and determine suitable locations for f_1 and f_2 such that the compensated bode plot crosses the unity gain axis at about the mid point of the -6db/octave line segment connecting f_1 and f_2. Selecting $f_1 = 1.5$hZ, and $f_2 = 7.0$HZ we have; (see Fig. 4)

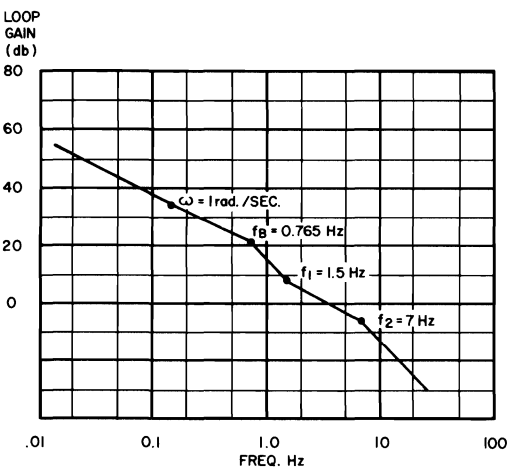


Fig. 4

$$f_1 = \frac{1}{2\pi R_2 C_2} = 1.5 \text{ HZ}$$

$$f_2 = \frac{C_2 + C_3}{2\pi R_2 C_2 C_3} = 7.0 \text{ HZ}$$

$$\frac{f_1}{f_2} = \frac{C_3}{C_2 + C_3} = 0.214$$

$C_3 = .214\,(C_2 + C_3)$

From Equation 10

$C_2 + C_3 = 11.74C_1 = .1174$uF

$C_3 = (.214)(.1174) \doteq 0.025$uF

Select $C_3 = .022$uf

and $C_2 = 0.1$uf

Then;

$$R_2 = \frac{1}{2\pi f_1 C_2} = 1M\Omega$$

Resistors R_3 and R_4 are chosen to bias the on-chip drive transistor in a linear region at the desired motor speed. To maintain closed loop stability of the integrator we keep the inverting gain of this stage close to unity. For this application $R_3 = 570\Omega$ and $R_4 = 1000\Omega$. A 470Ω resistor is selected for R_5 to provide sufficient zener bias from the 12V supply. The component list for the circuit in Figure 2B is:

R_1	$146K\Omega$	C_1	0.01uf
R_2	$1M\Omega$	C_2	0.1uf
R_3	510Ω	C_3	0.022uf
R_4	1000Ω		
R_5	470Ω		
P_1	$100K\Omega$		

This design example illustrates a method for computing component values to insure closed loop stability of the motor speed regulator system. It is based on an application circuit which includes an integrator to provide for zero steady state error under varying load conditions. This system, with loop gain equal to 50 at ω equal 1 RAD/Sec gave acceptable static and dynamic performance for the intended application.

5

ABSOLUTE MAXIMUM RATINGS

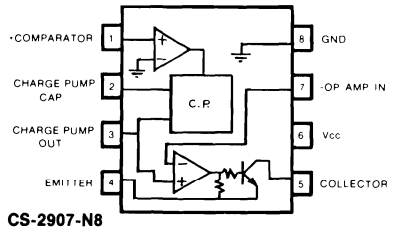
Supply Voltage	28V
Supply Current	25mA
Op. Amp./Comp. Differential Input Voltage	28V
Op. Amp./Comparator Input Voltage	28V
Op. Amp. Collector-Emitter Voltage	28V
Digital Interface Collector-Emitter Voltage	28V
Operating Temperature Range	-40° C to +85° C
Storage Temperature Range	-65° C to +150° C
Power Dissipation	1 Watt Note 1

NOTES:
1. Above 25° Derate at 8.0mW/° C for package D14 and at 10.0mW/° C for package D8.
2. Hysteresis is the sum +VTH-(VTH), offset voltage is their difference.
3. V_{OH} is equal to ¾ x V_{cc} - 1 V_{BE}, V_{OL} is equal to ¼ x V_{cc} - 1 V_{BE} therefore V_{OH} - V_{OL} = $V_{cc}/2$. The difference, V_{OH} - V_{OL}, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.
4. Be sure when choosing the time constant R1 x C1 that R1 is such that the maximum anticipated output voltage at Pin 3 can be reached with I_3 x R1. The maximum value for R1 is limited by the output resistance of Pin 3 which is greater than 10MΩ typ.
5. Nonlinearity is defined as the deviation of Vout (@ Pin 3) for fIN = 5kHz from a straight line defined by the Vout @ 1kHz and Vout @ 10kHz, C1 = 1000pF, R1 = 68K and C2 = 0.22uFd.

SPECIFICATIONS (T_a = 25° C and V_{cc}=12VDC unless otherwise noted)

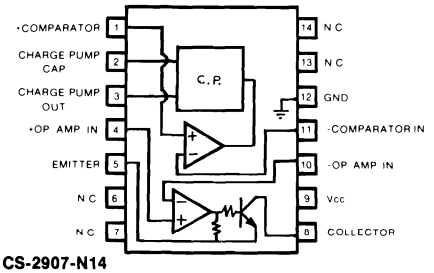
PARAMETER		CONDITIONS		MIN.	TYPICAL	MAX.
COMPARATOR						
Input Threshold Voltage		V_{pin1}=±125mV	Note 2	±10mV	±15mV	±40mV
Hysteresis		V_{pin1}=±125mV	Note 2		30mV	
Input Offset Voltage	—D14 Versions	Note 2			3.5mV	10mV
* * *	—D8 Versions	Note 2			5mV	15mV
Input Bias Current		V_{pin1}=±50mV			0.1μA	1.0μA
Common Mode Voltage						V_{cc}—1.5V
DIGITAL INTERFACE (—1 Versions Only)						
Saturation Voltage (Pin 13)		$I_{pin\ 13}$=1.6mA				0.4V
CHARGE PUMP						
Output Voltage - HI, V_{oh}	CS-2907 Series	V_{pin1}=+125mVDC	Note 3		8.3V	
* * *	CS-2917 Series	V_{pin1}=+125mVDC	Note 3		5V	
Output Voltage - LO, V_{ol}	CS-2907 Series	V_{pin1}=—125mVDC	Note 3		2.3V	
* * *	CS-2917 Series	V_{pin1}=—125mVDC	Note 3		1.2V	
Output Current I_{pin2}; I_{pin3}	CS-2907 Series	V_{pin2}=V_{pin3}=6VDC	Note 4	140μA	180μA	240μA
* * * *	CS-2917 Series	V_{pin2}=V_{pin3}=3.5VDC; V_{cc}=6VDC	Note 4	120μA	160μA	215μA
Leakage Current I_{pin3}		I_{pin2}=0; V_{pin3}=0				0.1μA
Gain Constant K		Note 3		0.9	1.0	1.1
Non-Linearity		Note 5		—1.0%	±0.3%	+1.0%
OP. AMP.						
Input Offset Voltage	CS-2907 Series	V_{input}=6VDC			3mV	10mV
* * *	CS-2917 Series	V_{input}=3.5VDC			3mV	10mV
Input Bias Current	CS-2907 Series	V_{input}=6VDC			.05μA	0.5μA
* * *	CS-2917 Series	V_{input}=3.5VDC			.05μA	0.5μA
Common Mode Voltage				0V		V_{cc}—1.5V
Open Loop Gain					200V/mV	
I_{sink}		$V_{collector}$=1V		40mA	50mA	
I_{source}	CS-2907 Series	$V_{emitter}$=V_{cc}—2V			10mA	
*	CS-2917 Series	$V_{emitter}$=V_{cc}—2V; V_{cc}=6VDC			10mA	
Saturation Voltage		I_{sink}=5mA			0.1V	0.5V
		I_{sink}=20mA				1.0V
		I_{sink}=50mA			1.0V	1.5V
ZENER REGULATOR (CS-2917 Series Only)						
Regulator Voltage		Dropping Resistor=470Ω			7.56V	
Series Resistance					10.5Ω	15Ω
Temperature Stability					+1mV/°C	
SUPPLY						
Current, Quiescent	CS-2907 Series	V_{cc}=12VDC			3.8mA	6.0mA
* *	CS-2917 Series	V_{cc}= 6 VDC		3.0mA	6.0mA	

AVAILABLE CONFIGURATIONS:



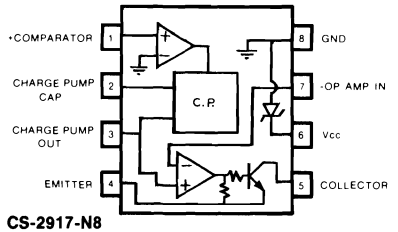
CS-2907-N8

8 Lead PDIP



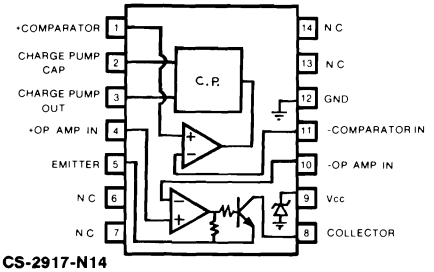
CS-2907-N14

14 Lead PDIP



CS-2917-N8

8 Lead PDIP



CS-2917-N14

14 Lead PDIP

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-2907N14	14 Lead PDIP
CS-2907N8	8 Lead PDIP
CS-2917N14	14 Lead PDIP
CS-2917N8	8 Lead PDIP

5

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-3717A

STEPPER MOTOR DRIVER

DESCRIPTION

The CS-3717A is a monolithic IC that controls and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three steps by means of two logic inputs which select one of three current comparators. When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow. A monstable, programmed by an external RC network, sets the current decay time.

The power section is a full H-bridge driver with four internal clamp diodes for current recirculation. An external connection to the lower emitters is available for the insertion of a sensing resistor. Two CS-3717A's and few external components form a complete stepper motor drive subsystem.

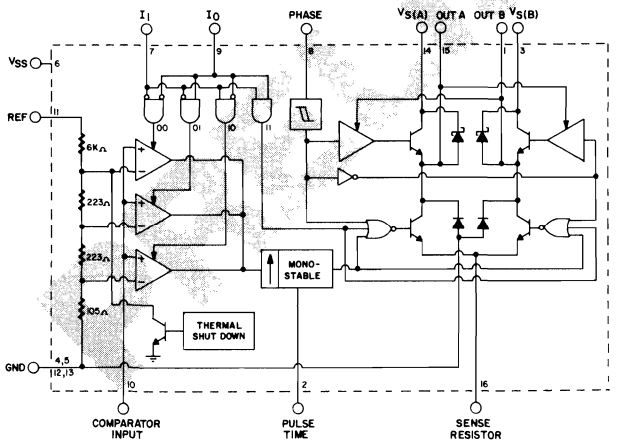
The recommended operating ambient temperature range is from 0 to 70°C.

The CS-3717A is supplied in a 16 lead Powerdip package.

ABSOLUTE MAXIMUM RATINGS

V_S	Power supply voltage (pins 14, 3)	50 V
V_{SS}	Logic supply voltage (pin 6)	7 V
V_I	Logic input voltage (pins 7, 8, 9)	6 V
V_C	Comparator input (pin 10)	V_{SS}
V_r	Reference input voltage (pin 11)	15 V
I_O	Output current (DC operation) CS-3717A	1.2 A
T_{stg}	Storage temperature	-55 to +150 °C
T_j	Operating junction temperature	150 °C

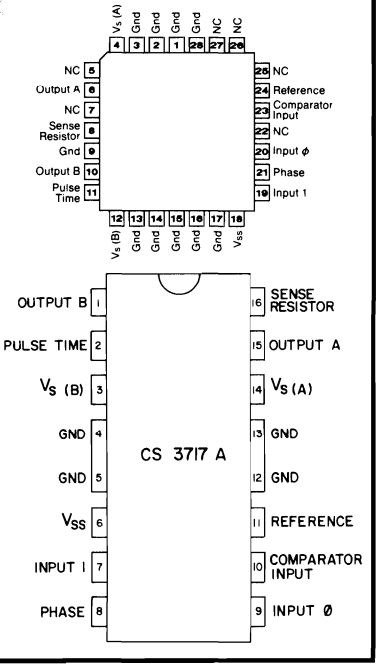
BLOCK DIAGRAM



FEATURES:

- Full Step - Half Step -Quarter Step Operation
- Bipolar Output Current Up To 1 Amp
- Motor Supply Voltage Range From 10V To 46V
- Integrated Bootstrap Lowers Saturation Voltage
- Built In Protection Diodes
- Externally Selectable Current Level
- Digital Or Analog Control Of Output Current Level
- Thermal Overload Protection
- Minimum External Components

PIN CONNECTIONS (TOP VIEW)



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS (Refer to the test circuit V_s=36V, V_{ss}=5V, T_{amb}=25°C unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Supply voltage (pins 3, 14)			10		46	V
V_{SS}	Logic supply voltage (pin 6)			4.75		5.25	V
I_{SS}	Logic supply current (pin 6)				7	15	mA
I_R	Reference input current (pin 11)	V_R=5V			0.75	1	mA
LOGIC INPUTS							
V_{IL}	Input low voltage (pins 7, 8, 9)					0.8	V
V_{IH}	Input high voltage (pins 7, 8, 9)			2		V_{SS}	V
I_{IL}	Low voltage input current (pins 7, 8, 9)	V_I=0.4V	pin 8			-100	μA
			pins 7.9			-400	μA
I_{IH}	High voltage input current (pins 7, 8, 9)	V_I=2.4V				10	μA
COMPARATORS							
V_{CL}	Comparator low threshold voltage (pin 10)	V_R=5V	I_0=L I_1=H	66	80	94	mV
V_{CM}	Comparator medium threshold voltage (pin 10)	V_R=5V	I_0=H I_1=L	236	251	266	mV
V_{CH}	Comparator high threshold voltage (pin 10)	V_R=5V	I_0=L I_1=L	396	416	436	mV
I_C	Comparator input current (pin 10)					±20	μA
t_{off}	Cutoff time	R_T=56 KΩ	C_T=820 pF	27		37	μs
t_d	Turn off delay	(See fig. 2)				2	μs
I_{off}	Output leakage current (pins 1, 15)	I_0=H I_1=H				100	μA
SOURCE DIODE-TRANSISTOR PAIR							
V_{sat}	Saturation voltage (pins 1, 15) (note 1)	I_M=-0.5A (See fig. 2)	conduction period		1.7	2.1	V
			recirculation period		1.1	1.35	
V_{sat}	Saturation voltage (pins 1, 15) (note 2)	I_M=-1A (See fig. 2)	conduction period		2.1	2.8	V
			recirculation period		1.7	2.5	
I_{LK}	Leakage current	V_s=46V				300	μA
V_F	Diode forward voltage	I_M=-0.5A			1	1.25	V
		I_M=-1A			1.3	1.7	
SINK DIODE-TRANSISTOR PAIR							
V_{sat}	Saturation voltage (pins 1, 15)	I_M=0.5A			1.2	1.45	V
		I_M=1A			1.75	2.3	
I_{LK}	Leakage current	V_s=46V				300	μA
V_F	Diode forward voltage	I_M=0.5A			1.1	1.5	V
		I_M=1A			1.4	2	

5

TRUTH TABLE

Input 0 (pin 9)	Input 1 (pin 7)	
H	H	No current
L	H	Low current
H	L	Medium current
L	L	High current

PIN DESCRIPTIONS

PIN NO.	FUNCTION	DESCRIPTION
1	OUTPUT B	Output connection (with pin 15). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
2	PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators (t_{off}=0.69 R_TC_T).
3	SUPPLY VOLTAGE B	Supply voltage input for half output stage. See also pin 14.
4	GROUND	Ground connection. With pins 5, 12 and 13 also conducts heat from die to printed circuit copper.
5	GROUND	See pin 4.
6	LOGIC SUPPLY	Supply voltage input for logic circuitry.
7	INPUT 1	This pin and pin 9 (INPUT 0) are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
8	PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
9	INPUT 0	See INPUT 1 (pin 7).
10	COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter R_cC_c. The lower power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R_TC_T, t_{off}=0.69 R_TC_T.
11	REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators, thus determining the output current (also dependent on R_s and the two inputs INPUT 0 and INPUT 1).
12	GROUND	See pin 4.
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE A	Supply voltage input for half output stage. See also pin 3.
15	OUTPUT A	See pin 1.
16	SENSE RESISTOR	Connection to lower emitters of output stage for insertion of current sense resistor.

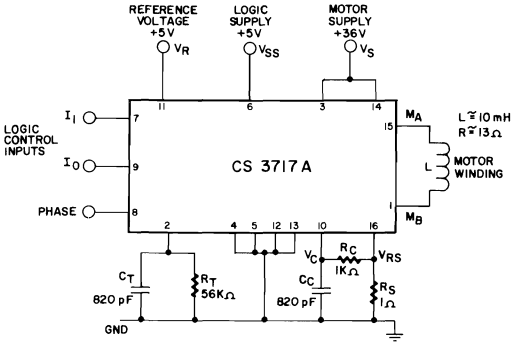


Figure 1 - Test Circuit

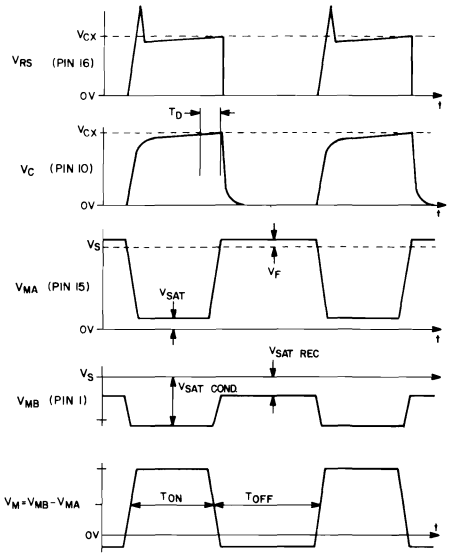


Figure 2 - Waveforms with MA regulating (phase = 0)

5

APPLICATION CIRCUIT

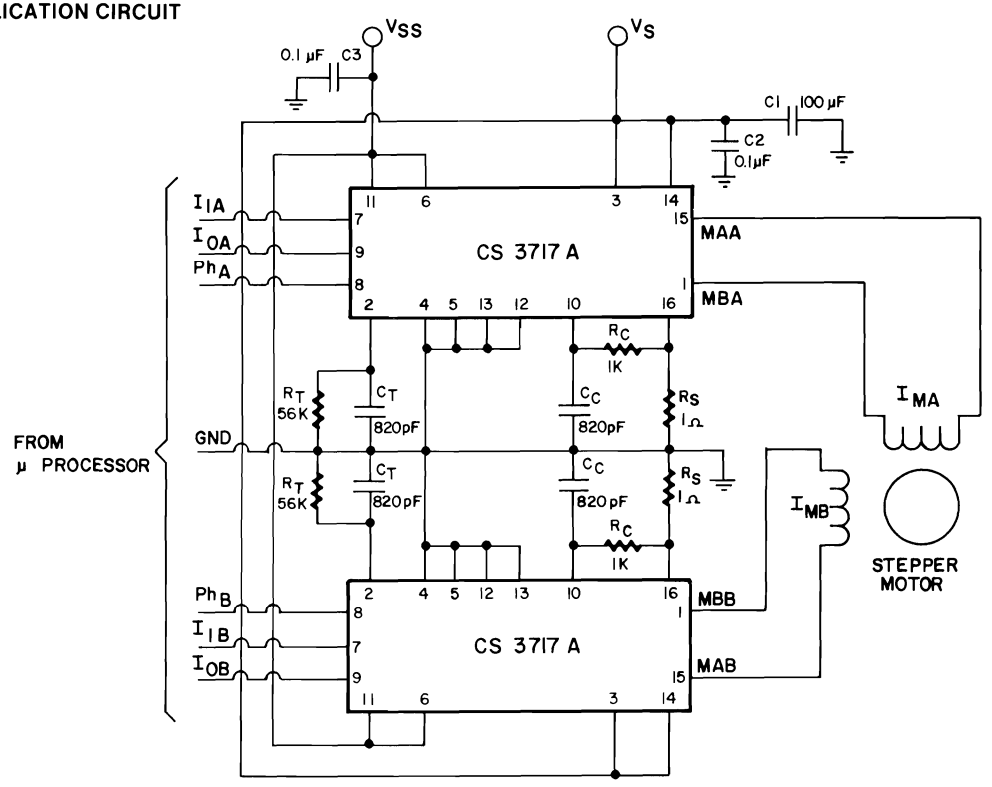


Figure 3 - Two phase bipolar stepper motor driver

Figure 3 shows a typical application in which two CS-3717A control a two phase bipolar stepper motor.

Programming

The logic inputs I_0 and I_1 set at three different levels the amplitude of the current flowing in the motor winding according to the truth table of page 2. A high level on the "PHASE" logic input sets the direction of that current from output A to output B; a low level from output B to output A.

It is recommended that unused inputs are tied to pin 6 (V_{SS}) or pin 4 (GND) as appropriate to avoid noise problems.

The current levels can be varied continuously by changing the ref. voltage on pin 11.

Control of the motor

The stepper motor can rotate in either direction according to the sequence of the input signals. It is possible to obtain a full step, a half step and a quarter step operation.

Full step operation

Both windings of the stepper motor are energized all the time with the same current $I_{MA} = I_{MB}$.

I_0 and I_1 remain fixed at whatever torque value is required.

Calling A the condition with winding A energized in one direction and $\overline{A}$ in the other direction, the sequence for full step rotation is:

$$AB \rightarrow \overline{A}B \rightarrow \overline{A}\,\overline{B} \rightarrow A\overline{B} \text{ etc.}$$

For rotation in the other direction the sequence must be reversed.

In full step operation the torque is constant each step.

Half step operation

Power is applied alternately to one winding then both according to the sequence:

$$AB \rightarrow B \rightarrow \overline{A}B \rightarrow \overline{A} \rightarrow \overline{A}\,\overline{B} \rightarrow \overline{B} \rightarrow A\overline{B} \rightarrow A \text{ etc.}$$

Like full step this can be done at any current level; the torque is not constant but is lower when only one winding is energized.

A coil is turned off by setting I_0 and I_1 both high.

Quarter step operation

It is preferable to realize the quarter step operation at full power otherwise the steps will be of very irregular size.

The extra quarter steps are added to the half step sequence by putting one coil on half current according to the sequence:

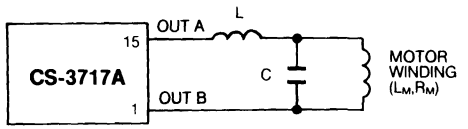
$$AB \rightarrow \frac{A}{2}B \rightarrow B \rightarrow \frac{\overline{A}}{2}B \rightarrow \overline{A}B \rightarrow \overline{A}\frac{B}{2} \rightarrow \overline{A} \text{ etc.}$$

Motor selection

As the CS-3717A provides constant current drive with a switching operation, care must be taken to select stepper motors with low hysteresis losses to prevent motor overheating.

L-C filter

To reduce EMI and chopping losses in the motor, a low pass L-C filter can be inserted across the outputs of the CS-3717A as shown in the following diagram.



$$L \cong \frac{1}{10} L_M \qquad C \cong \frac{4 \cdot 10^{10}}{L}$$

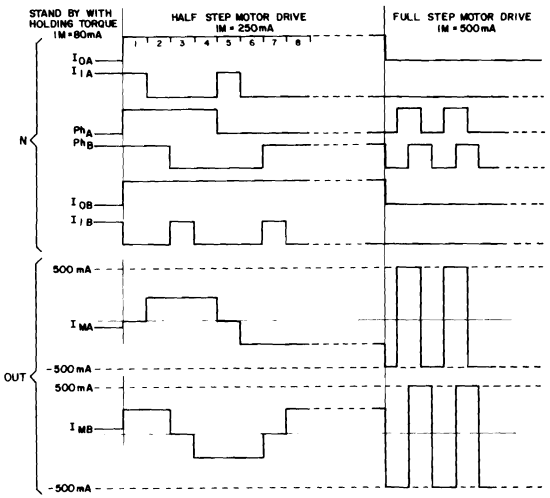


Fig. 4 - Input and output sequences for half step and full step operation

Fig. 5 - Source Saturation Voltage vs. Output Current (Recirc. Period)

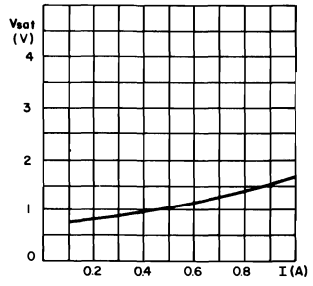


Fig. 6 - Source Saturation Voltage vs. Output Current (Conduction Period)

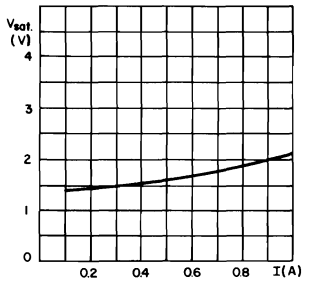


Fig. 7 - Sink Saturation Voltage vs. Output Current

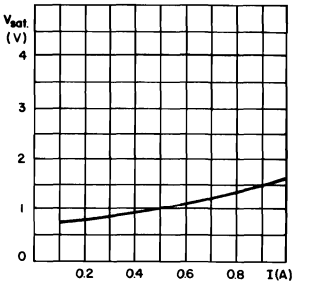


Fig. 8 - Comparator Threshold vs. Junction Temperature

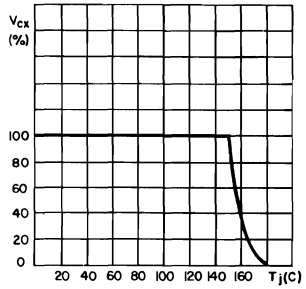


Fig. 9 - Example Of P.C. Board Copper Area Which Is Used As Heatsink

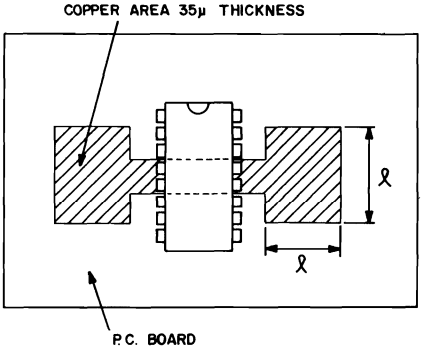
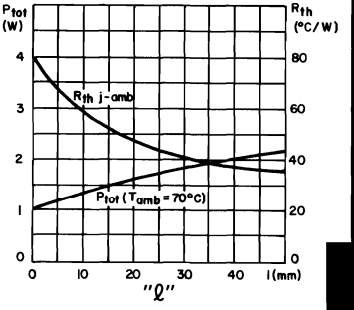


Fig. 10 - Max. Power Dissipation And Junction To Ambient Thermal Resistance vs. Size "ℓ"



5

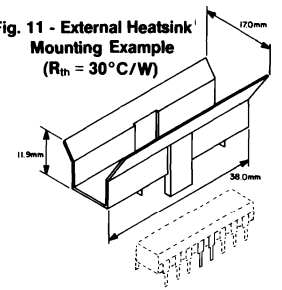
MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the CS-3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of fig. 10 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (see fig. 9). In addition, it is possible to use an external heatsink (see fig. 11). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 11 - External Heatsink Mounting Example (R_{th} = 30°C/W)

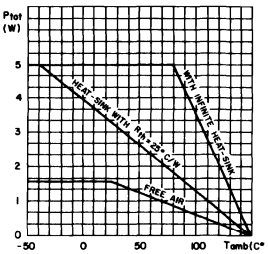


THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	11	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient*	40	°C/W

*Soldered on a 35μ thick 20 cm² P.C. board copper area

Fig. 12 - Maximum Allowable Power Dissipation vs. Ambient Temperature



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-3717AN	16 Lead PDIP
CS-3717AFN	28 Lead PLCC

CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-3770

HIGH PERFORMANCE STEPPER MOTOR DRIVER

DESCRIPTION

The CS-3770 is a bipolar monolithic circuit intended to control and drive the current in one winding of a stepper motor. Special care has been taken to optimize the power handling capability without suffering in reliability.

The circuit consists of a LS-TTL compatible logic input, a current sensor, a monostable multivibrator and a high power H-bridge output stage.

Two CS-3770's and a small number of external components form a complete control and drive unit for LS-TTL or microprocessor controlled stepper motor systems.

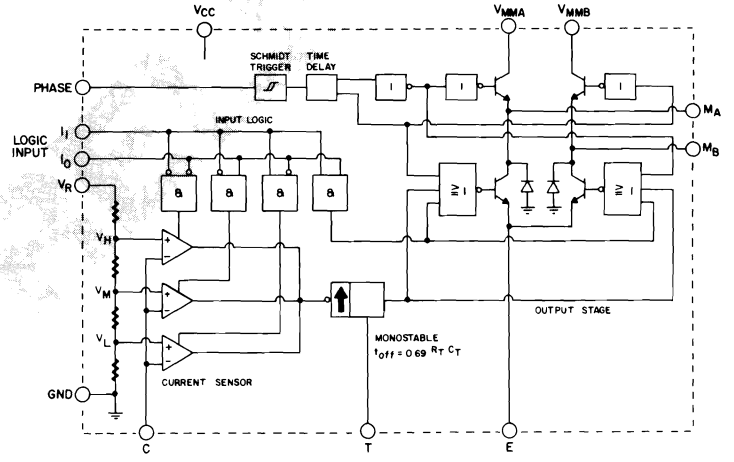
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Units
Logic Supply Voltage	V_{cc}	7	V
Output Supply Voltage	V_{mm}	45	V
Logic Input Voltage		6	V
Comparator Input Voltage		V_{cc}	V
Reference Input Voltage		15	V
Logic Input Currents		-10	mA
Comparator Input Current		-10	mA
Reference Input Current		-10	mA
Output Current		±1.5	A
Junction Temperature	T_j	150	°C
Operating Ambient Temperature	T_A	0 to + 70	°C
Storage Temperature	T_S	-55 to +150	°C

FEATURES:

- Half-step and full-step modes
- Switched mode bipolar constant current drive (chopped mode)
- Wide range of current control 5—1500 mA
- Wide voltage range 10—45 V
- Designed for unstabilized motor supply voltage
- Current levels can be selected in steps or varied continuously
- Thermal overload protection
- LS-TTL compatible input logic
- Available in a 16L plastic power dip and a 28L PLCC

BLOCK DIAGRAM CS-3770N



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Logic Supply Voltage	V_{cc}	4.75	5	5.25	V
Output Supply Voltage	V_{mm}	10		40	V
Output Current	I_m	20		1200	mA
Ambient Temperature	T_a	0		70	°C
Rise Time Logic Inputs	tr			2	μs
Fall Time Logic Inputs	tf			2	μs

ELECTRICAL CHARACTERISTICS

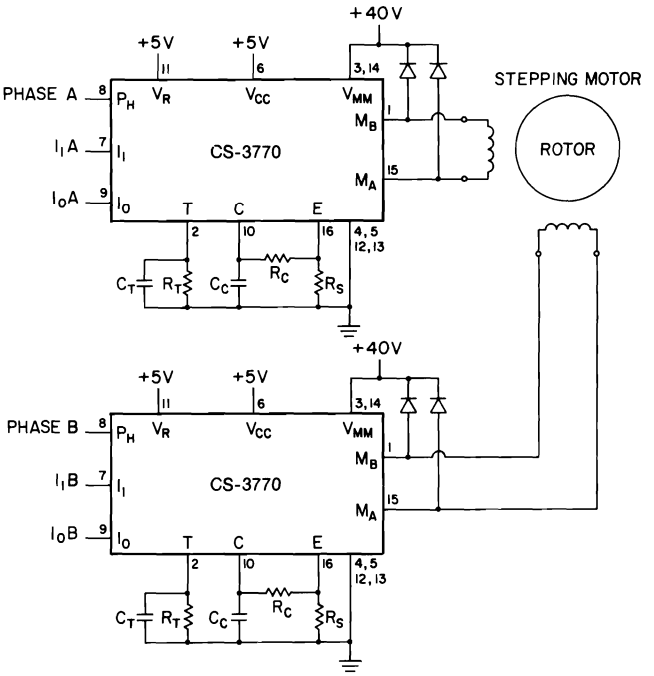
Electrical characteristics over recommended operating conditions 0° to 70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, I_{CC}	V_{MM} = 20–40 V $I_1 = I_0 = 1$ $I_1 = I_0 = 0$		20 65	30 145	mA mA
High-level logic input voltages pins 7, 8, 9		2.0			V
Low-level logic input voltages				0.8	V
High-level logic input currents pins 7, 8, 9	V_I = 2.4 V			20	μA
Low-level logic input currents	V_I = 0.4V	-0.4			mA
Comparator threshold voltage	$I_0 = 0$ V_R = 5.0 V $I_1 = 0$	390	420	440	mV
	$I_0 = 1$ V_R = 5.0 V $I_1 = 0$	230	250	270	mV
	$I_0 = 0$ V_R = 5.0 V $I_1 = 1$	65	80	90	mV
Comparator input current		-20		20	μA
Output leakage current	$I_0 = I_1 = 1$; T_a = 25°C			100	μA
Total saturation voltage drop (source + sink)	I_m = 800 mA			2.0	V
Total power dissipation	I_m = 800 mA fs = 30 kHz		1.8	*	W
Cut off time, t_{OFF}	R_T = 56KΩ, C_T = InF V_{mm} = 10V, $t_{on} \geq 5$ μS	35	40	45	μs
Turn off delay, t_d	T_a = +25°C $dV_C/dt \geq 50mV/\mu s$		1.6	3.0	μs
Thermal shutdown junction temp			+170		°C

* Depends upon heat sink (see Fig. 3 & Fig. 9)

5

TYPICAL APPLICATION



Test Circuit
R_T=56KΩ
C_T=820pf
R_S=0.5Ω±1%
R_C=1KΩ
C_C=820pf

Fig. 1 Typical stepper motor driver with CS-3770N

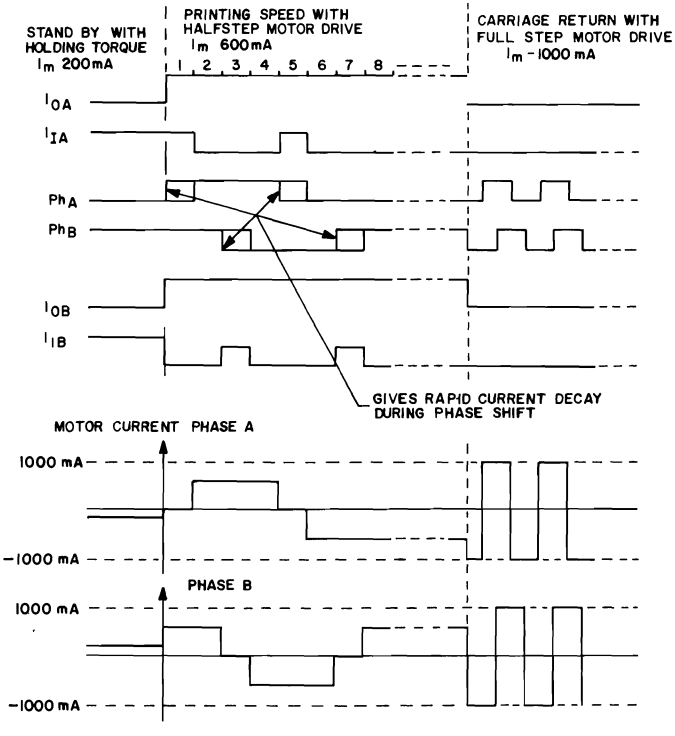


Fig. 2 Principal Operating Sequence

Functional Description

Current Level Selection
The status of I_0 and I1 input pins in conjunction with the reference voltage V_{ref} determines the output current. If V_{ref} is fixed four current levels can be selected:

LOGIC I_0	INPUT I1	CURRENT LEVEL Imotor
H	H	No Current
L	H	Low (20%) Current
H	L	Medium (60%) Current
L	L	High (100%) Current

Sense Resistor
The voltage drop across the current sensing resistor , Rs, is compared with the voltage drop across reference resistor chain (using Vref). When the two values are equal the monostable is triggered which in turn sets the output in tristate for a fixed time Toff (Toff=0.69 x Rt x Ct). The Rc-Cc network is a filter for the sensing resistor Rs.

Output Stage
The output contains four power transistors connected in an H-bridge. The lower two sink transistors have diodes across them. It is recommended to use two external diodes across the two upper source transistors when driving inductive load.

Reference Voltage
Variation of Vref can give wide control of motor current. A modulated Vref provides continuously adjusted motor current (for example, when microstepping the motor).

Phase Input
At Phase input pin a logic signal determines the direction of current in the motor winding. A Schmitt triger provides noise immunity and a delay circuit eliminates the possibility of output short circuit during a phase shift.

Thermal Protection
A thermal shut down is provided which limits the junction temperature. However, there is no short circuit protection.

Thermal data

	Typ	Unit
Thermal resistance, Junction to Case 0_{jc}	11	°C/W
Thermal resistance, Junction to Ambient 0_{jc}	45	°C/W

(Soldered on a 35μm thick 20 cm² PC board copper area)

Heatsinking

The junction temperature of the chip highly affects the lifetime of the driver circuit. Thus in high current applications the heatsinking must be carefully considered.

The θ_{ja} of the CS-3770 can be reduced by soldering the GND-pins to a suitable copper area on the printed circuit board (see fig. 7) or by applying an external heatsink Staver type V7 or V8 (see fig. 8). The diagram in figure 3 shows the maximum permissible power dissipation versus the ambient temperature in °C, for heatsinkers of the type V7, V8 or fig. 7 for a 20 cm² copper area respectively. Any external heatsink or printed circuit board copper area must be connected to electrical ground. For motor currents higher than 1000 mA heatsinking is recommended to assure optimal reliability.

The diagrams in fig. 3 and fig. 6 can be used to determine the required heatsinking of the circuit. In some systems forced air cooling may be available to reduce the temperature rise of the circuit.

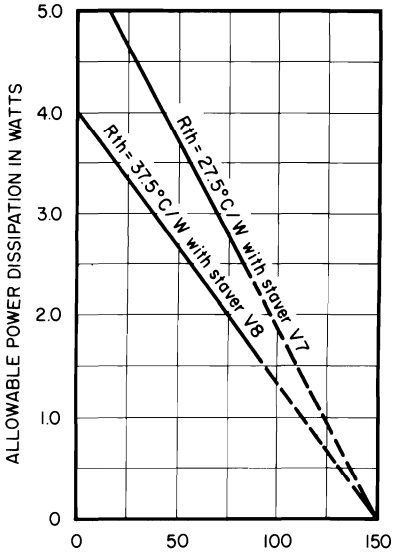


Fig. 3 Ambient temperature in °C.

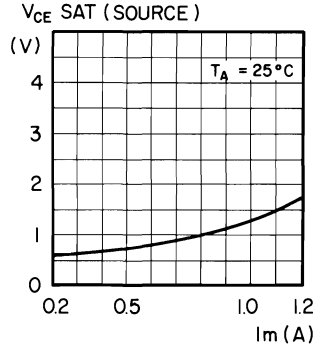


Fig. 4 Typical source saturation voltage vs output current.

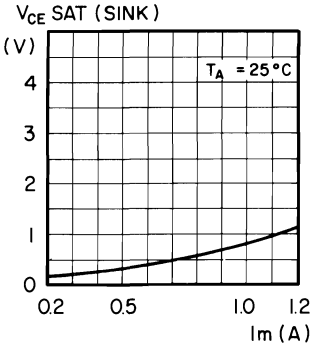


Fig. 5 Typical sink saturation voltage vs output current.

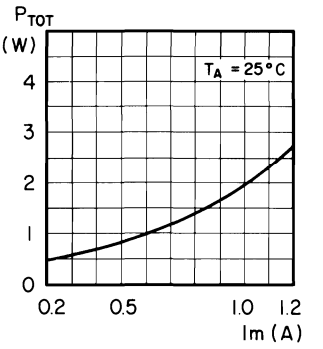


Fig. 6 Typical power losses vs output current.

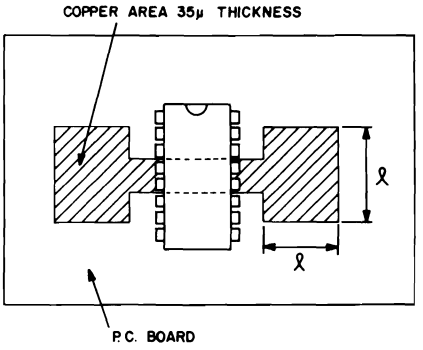
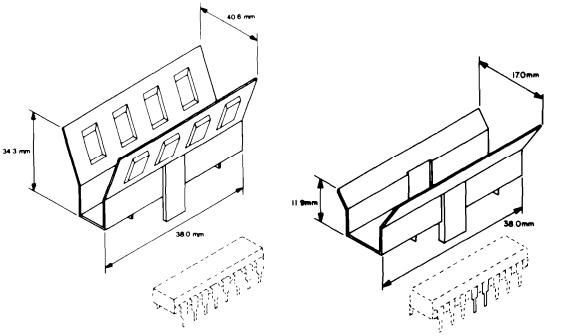


Fig. 7 Example Of P.C. Board Copper Area Which Is Used As Heatsink.



TYPE V7 **TYPE V8**

Fig. 8 External Heatsink Mounting Example
(R_{th} = 27.5°C/W) (Type V7)
(R_{th} = 37.5°C/W) (Type V8)

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the CS-3770 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of fig. 9 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (see fig. 7). In addition, it is possible to use an external heatsink (see fig. 8). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The printed circuit copper area must be connected to electrical ground.

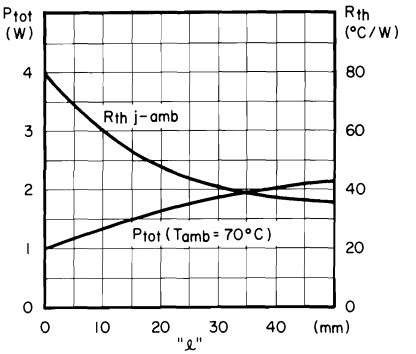
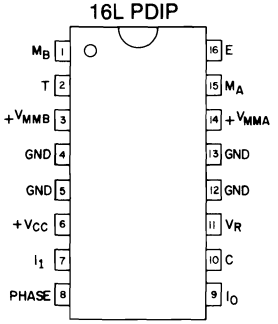


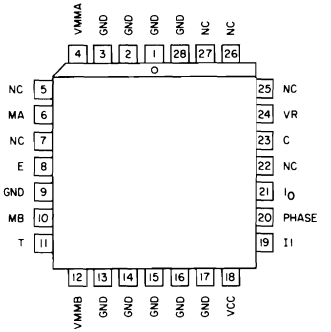
Fig. 9 Max. Power Dissipation And Junction To Ambient Thermal Resistance vs Size "ℓ"

Pin Connections and Ordering Information

16L PDIP



28L PLCC



ORDERING INFORMATION

PART NUMBER	PACKAGE
CS-3770N	16 Lead PDIP
CS-3770FN	28 Lead PLCC

CSC™ CHERRY SEMICONDUCTOR

CS-189

TACHOMETER DRIVE CIRCUIT

DESCRIPTION

The CS-189 is specifically designed for use with air-core meter movements. The IC (see Block Diagram, Figure 1) comprises charge pump circuitry for frequency-to-voltage conversion, a shunt regulator for stable operation, a function generator, and sine and cosine amplifiers. The buffered sine and cosine outputs will typically sink or source 20mA.

CHARGE PUMP

The input frequency is buffered though a transistor, then applied to the charge pump for frequency-to-voltage conversion (see Functional Diagram, Figure 2). The charge pump output voltage, EØ, will range from 2.1V with no input (Ø=0°) to 7.1V at Ø=270°. The charge that appears on C_T is reflected to C_{OUT} through a Norton amplifier. The frequency applied at Pin 10 charges and discharges C_T through R_1 and R_2. C_{OUT} reflects the charge as a voltage across resistor R_T.

FUNCTION GENERATOR/SINE AND COSINE AMPLIFIERS

The output waveforms of the sine and cosine amplifiers are derived by On-Chip Amplifier/Comparator circuitry. The various trip points for the circuit (i.e. 90°, 180°, 270°) are determined by an internal resistor divider connected to the voltage regulator. The voltage EØ is compared to the divider network by the function generator circuitry. Use of an external zener reference at Pin 1 allows both sine and cosine amplifiers to swing positive and negative with respect to this reference. The output magnitudes and directions have the relationship as shown in Figures 3A, 3B and 3C.

NOTE: Pin connections referenced are for the 14L DIP

BLOCK DIAGRAM

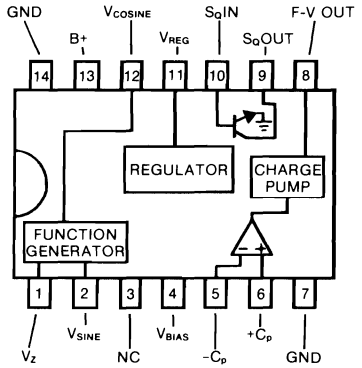
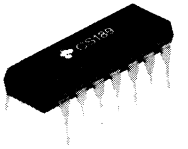


FIGURE 1

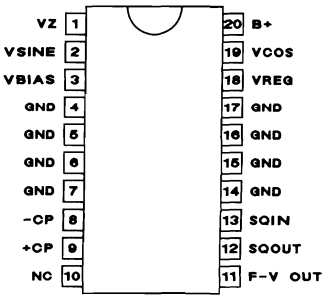


FEATURES:
- Single supply operation
- On-Chip regulation
- 20mA output drive capability
- Wide temperature range
- Accuracy = .05%/°C

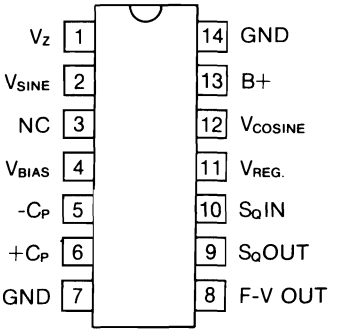
APPLICATIONS:
- Tachometers
- Speedometer
- F/V conversion
- Windspeed & direction
- Flowmeter control

PIN CONNECTIONS

20L SOIC WIDE



14L DIP



(TOP VIEW)

6

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... -30° C to +100° C
Storage Temperature ..... -65° C to +150° C
Supply Voltage 20V
Power Dissipation ..... 2W@ 25° C
(Derate 16mW/° C above 25° C)

ELECTRICAL CHARACTERISTICS (V_{CC}=13.1V, T_A=25° C)

PARAMETER	SYMBOL	PIN NO.	TEST CONDITIONS (SEE TEST CIRCUIT FIG. 1)	MIN.	TYP.	MAX.	UNITS
Supply Current (note 2)	1_{CC}	13	V_{CC}=15V		54	72	mA
			V_{CC}=13.1V		45	60	
			V_{CC}=11.3V		38	60	
Regulated Voltage	V_{REG}	11	I_{REG}=4.3mA	7.8	8.5	9.2	V
Regulation	ΔV_{REG}		I_{REG}=0 to 5mA		0.10	0.20	
Signal Input Current	I_{IN}	10		0.1	2.0	4.0	mA
Saturation Voltage	V_9SAT	9	I_9=5mA, I_{10}=0.5mA		0.20	0.40	V
Leakage Current	I_9		V_9=16V, V_{10}=0V			10	μA
Input Current	I_5	5	Zero input to pin 6		1	15	nA
Input Current	I_6	6					
F to V Output	E MIN	8	V_{10}=0 (zero input), ∅=0°	1.9	2.1	2.3	V
	E MAX		V_{COS}=0 (note 1), ∅=270°	6.6	7.1	7.6	
Linearity	%	8	E_O vs. Frequency V_{COS}=0 (note 1), ∅=270°			±1.5	%
V_{SINE} at ∅=0°	V_{SINE}	2	V_{10}=0 (zero input), ∅=0°	-0.35	0	+0.35	V
MAX V_{SINE} +			V_{COS}=0 (note 1), ∅=90°	4.0	4.5	5.0	
MAX V_{SINE} -			V_{COS}=0 (note 1), ∅=270°	-4.0	-4.5	-5.0	
Coil Drive Current	I_{SINE} +	2	V_{COS}=0 (note 1), ∅=90°		20	25	mA
	I_{SINE}-		V_{COS}=0 (note), ∅=270°		20	25	
MAX V_{COS}+	V_{COS}	12	V_{10}=0 (zero input), ∅=0°	4.0	4.5	5.0	V
MAX V_{COS}-			V_{SINE}=0 (note 1), ∅=180°	-4.0	-4.5	-5.0	
Coil Drive Current	I_{COS}+	12	V_{10}=0 (zero input), ∅=0°		20	25	mA
	I_{COS}-		V_{SINE}=0 (note 1), ∅=180°		20	25	
External Voltage Ref.	V_Z	1		5.13	5.40	5.67	V

Note 1: V_{SINE} measured Pin 2 to Pin 1. V_{COS} measured Pin 12 to Pin 1. All other voltages specified are measured to ground.
Note 2: Max PWR dissipation ≤ V_{CC} x I_{cc} -(V_2 I_{SINE} + V_{12} I_{COS}).

FUNCTION GENERATOR OUTPUT (∅): V_{CC}=13.1V, T_A=25° C

$$\varnothing = \text{ArcTan}\left(\frac{V_{sine}}{V_{co}}\right)$$ (Measured angle after calibration at 180° C)

For $\varnothing_A$=45°, 90°, 135°, 180°, 225°, 270°, (Desired angle)
($\varnothing_A$-$\varnothing_M$)≤4.0°

TEMPERATURE SENSITIVITY: V_{CC}=13.1V
$\Delta\varnothing_{MT}$=$\varnothing_M$ (T=25° C) -$\varnothing_M$ (-20° C≤T≤+85° C)
($\Delta\varnothing_{MT}$) ≤3.5° C, -20° C≤T≤+85° C

VOLTAGE SENSITIVITY: T_A=25° C
$\Delta\varnothing_{MV}$=$\varnothing_M$ (V_{CC}=13.1V) -$\varnothing_M$ (11.3V≤V_{CC}≤15V)
($\Delta\varnothing_{MV}$)≤2°, 11.3V≤V_{CC}≤15V

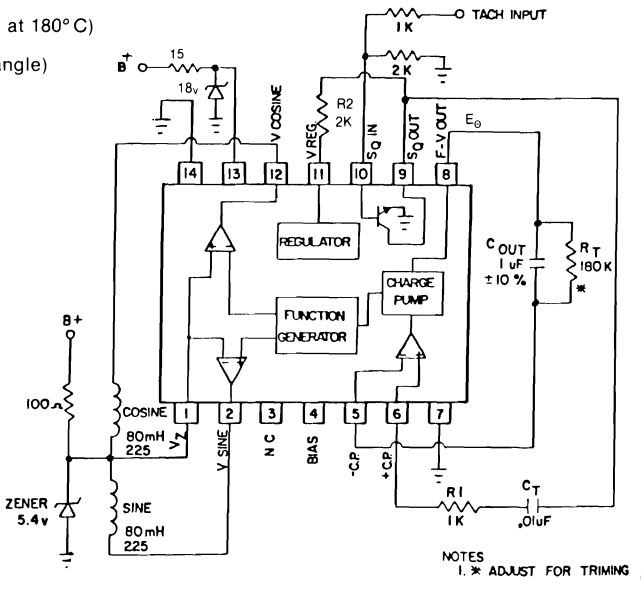


FIGURE 2
FUNCTIONAL DIAGRAM
(TEST CIRCUIT)

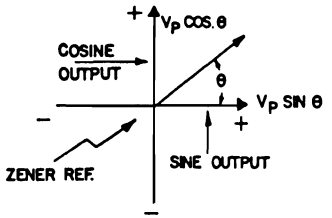


FIGURE 3A

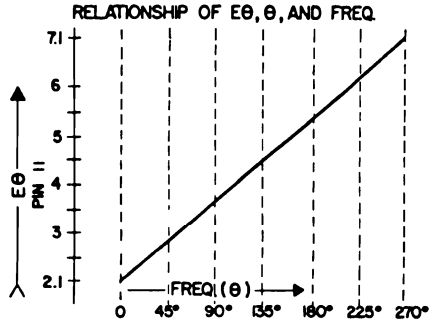


FIGURE 3B

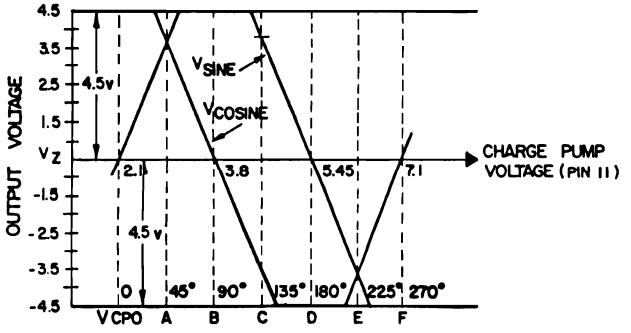


FIGURE 3C

TACHOMETER APPLICATION

$$\frac{RPM}{60} \times \frac{\#\ OF\ CYL.}{2} = Frequency$$

E (Pin 8)=2.1 + Frequency x C_T x R_T (V_{REG}-.7)

The above equations were used in calculating the following values, where E=7.1V at =270° and C_T=.01 F.

4 cylinder: Freq=200Hz, R_T=320K
6 cylinder: Freq=300Hz, R_T=220K
8 cylinder: Freq=400Hz, R_T=150K

Typical values shown above apply to a nominal value of V_{REG} of 8.5 volts. It must be realized that trimming of R_T will be necessary to compensate for variations in regulator voltage from one unit to another.

An alternative to this adjustment is to replace R_2 with a potentiometer, as shown in Figure 4.

Partial schematic shown in Figure 5 represents one method for use with DC applications instead of frequency.

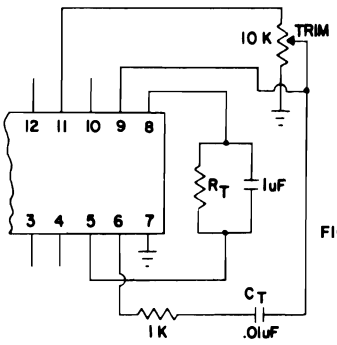


FIGURE 4

ALTERNATE TRIMMING METHOD

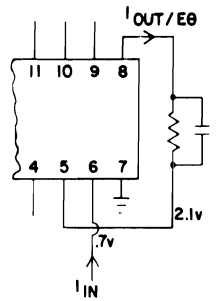


FIGURE 5

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-189DW	20 Lead SO Wide
CS-189N	14 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

CS-287
CS-288

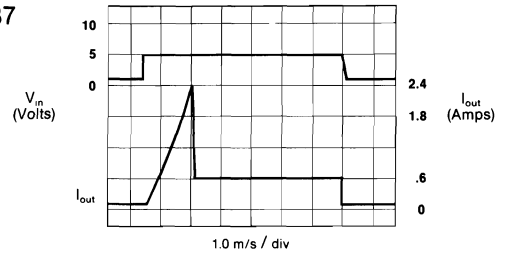
INJECTOR SOLENOID DRIVER

The CS-287/8 is a monolithic integrated circuit designed for medium current solenoid driver applications. Its typical function is to supply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening.

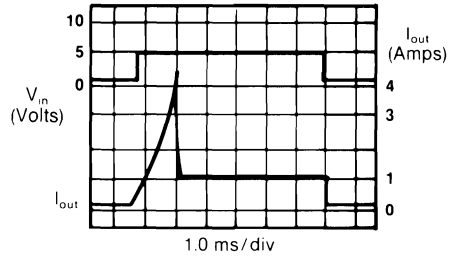
When load current reaches a preset level (2.4A for CS-287, or 4.4A for CS-288) the injector driver reduces the load current by a 4:1 ratio and operates as a constant power source. This condition holds the injector open and reduces system dissipation.

Other solenoid or relay applications can be equally well served by the CS-287/8. Two high impedance inputs are provided which permit a variety of control options and can be driven by TTL or CMOS logic.

CS287



CS288



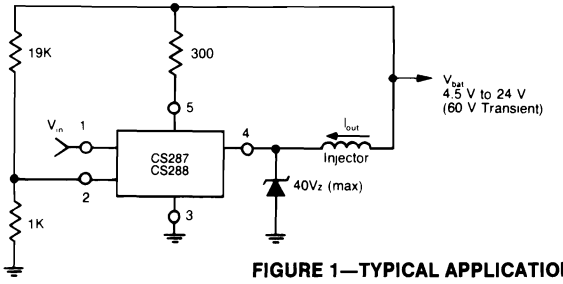
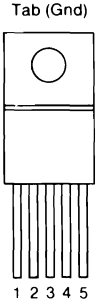


FIGURE 1—TYPICAL APPLICATION



PIN CONNECTIONS

1 Input
2 Control
3 Ground
4 Output
5 + V_{cc}

FEATURES:

- Microprocessor Compatible Inputs
- On-Chip Power Device
  2.4A Peak, Typical CS-287
  4.4A Peak, Typical CS-288
- Low Thermal Resistance To Grounded Tab
- Load Dump Safe
- Low Saturation Voltage
- Operates Over a 4V to 24V Battery Range

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

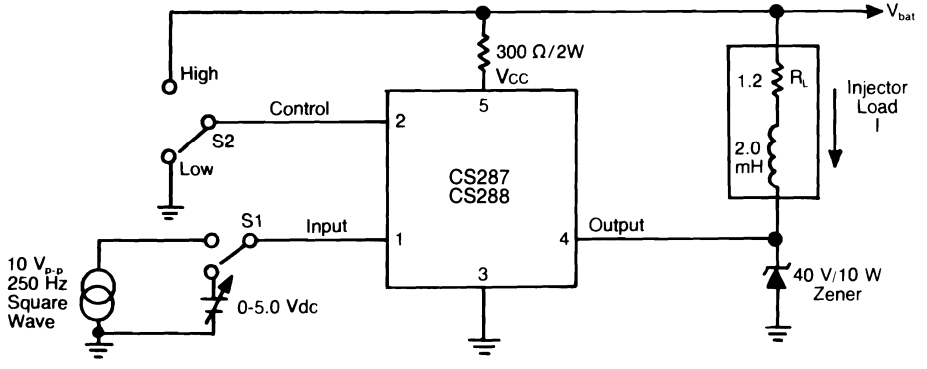
MAXIMUM RATINGS

RATING	VALUE	UNIT
Power Supply Voltage (V_{bat})	24	Volts
Input (Pin 1)	-6.0 to +24	V
Control (Pin 2)	-6.0 to +24	V
Internal Regulator Current (Pin 5)	50	mA
Junction Temperature	150	°C
Operating Temperature Range (Tab Temperature)	-40 to +125	°C
Storage Temperature Range	-65 to + 150	°C
Thermal Resistance, Junction to Case	3.0	°C/W

ELECTRICAL CHARACTERISTICS (V_{bat} = 12 Vdc, Tc = 25°C, test circuit of Figure 2, unless noted)

CHARACTERISTIC		MIN	TYP	MAX	UNITS
Output Peak Current (I_{pk})	287	1.7	2.4	2.9	A
	288	3.6	4.4	5.2	
Output Sustaining Current (I_{sus})	287	.50	.60	.70	A
	288	.95	1.12	1.25	
$V_{(BR)CEO(sus)}$ @ 100 mA		42	50	—	V
Output Voltage in Saturated Mode					
@ 1.5A		—	1.2	—	V
@ 3.0A		—	1.6	—	V
Internal Regulated Voltage (V_{cc}, Figure 2)		—	6.9	—	V
Input "on" Threshold Voltage		—	1.4	2.0	V
Input "off" Threshold Voltage		0.7	1.3	—	V
Input "on" Current					
@ V_I = 1.4 Vdc		—	35	—	μA
@ V_I = 5.0 Vdc		—	220	—	μA
Control "on" Threshold Voltage		1.2	1.5	1.8	V
Control Current					
@ V_2 = 0.8 Vdc		—	-5	-50	μA
@ V_2 = 5.0 Vdc		—	1.0	—	μA
Input Turn On Delay (t_i)		—	0.5	1.0	μs
I_{pk} sense to I_{sus} delay (t_p)		—	60	—	μs
Control Signal Delay (t_f)		—	15	—	μs
Input Turn Off from Saturated Mode Delay (t_e)		—	1.0	—	μs
Input Turn Off from Sustain Mode Delay (t_d)		—	0.2	—	μs
Output Voltage Rise Time (t_v)		—	0.4	—	μs
Output Current Fall Time (t_f) 4.0A		—	0.6	1.0	μs

FIGURE 2—TEST CIRCUIT



6

GENERAL INFORMATION

Inductive actuators such as automotive electronic fuel injectors, relays, solenoids and hammer drivers can be powered more efficiently by providing a high current drive until actuation (pull-in) occurs and then decreasing the drive current to a level which will sustain actuation. Pull-in and especially drop-out times of the actuators are also improved.

The fundamental output characteristic of the CS-287/8 provides a low impedance saturated power switch until the load current reaches a predetermined high-current level and then changes to a current source of lower magnitude until the device is turned off. This output characteristic allows the inductive load to control its actuation time during turn-on while minimizing power and stored energy during the sustain period, thereby promoting a fast turn-off time.

Automotive injectors at present time come in two types. The large throttle body injectors have an inductance of about 2.0 mH and an impedance of 1.2Ω and require the CS-287/8 driver. The smaller type, popular world-wide, has an inductance of 4.0 mH and an impedance of 2.4Ω and needs about a 2.0A pulse for good results, which can be met with the CS-287. Some designs are planned which employ two of the smaller types in parallel. The inductance of the injectors are much larger at low current, decreasing due to armature movement and core saturation to the values above at rated current.

Operating frequencies range from 5.0Hz to 250 Hz depending on the injector location and engine type. Duty cycle in some designs reaches 80%.

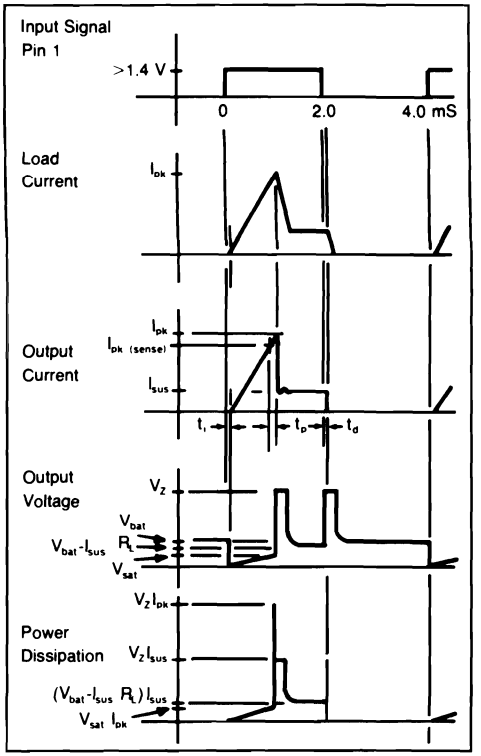
APPLICATIONS INFORMATION

The CS-287/8 is provided with an input pin (Pin 1) which turns the injector driver "on" and "off". This pin has a nominal trip level of 1.4 V and an input impedance of 20kΩ. It is internally protected against negative voltages and is compatible with TTL and most other logic.

There is also a control pin (Pin 2) which if held low or grounded, permits the device to operate in saturation to $I_{pk(sense)}$, where it will switch to I_{sus} automatically. If Pin 2 is brought high (>1.5V), the output drive stage is turned off, regardless of what state the input (Pin 1) is at, and the output current goes to zero.

Figure 3 shows the operating waveforms for the simplest mode; i.e., with control Pin 2 grounded. When the driver is turned on, the current ramps up to the peak current sense level, where some overshoot occurs because of internal delay. The CS-287/8 then reduces its output to I_{sus}. The fall time of the device is very rapid (≤1.0 μs), but the decay of the load current takes 150 to 220 μs, while dumping the load energy into the protection zener clamp.

FIGURE 3—OPERATING WAVEFORMS
(Max. Frequency 250 Hz, Pin 2 Grounded)



It is essential that the zener voltage be lower than the $V_{(BR)CEO(sus)}$, but not so low as to greatly stretch the load current decay time. Without the zener, the discharge of the load energy would be totally into the CS-287/8, which, for the high current applications, could cause the device to fail.

Also in Figure 3 is the graphically derived instantaneous power dissipation of the CS-287/8. It shows that, for practical purposes, the worst case dissipation is less than $(I_{sus})\ (V_{bat})$ (duty cycle).

FIGURE 4—SWITCHING WAVEFORMS
(Expanded Time Scale)

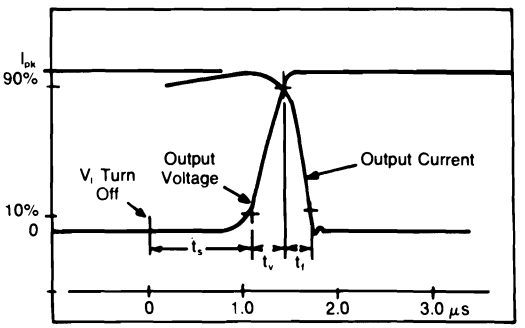


FIGURE 5—SWITCHING SPEED versus TEMPERATURE

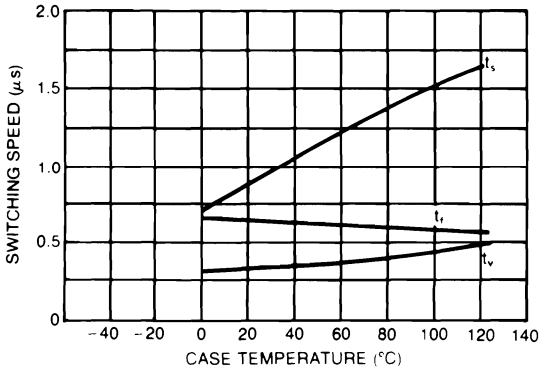
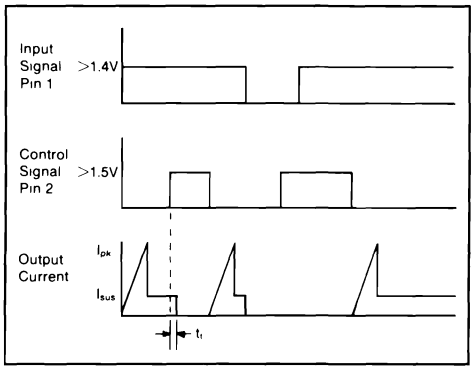


FIGURE 6—APPLICATION OF CONTROL (PIN 2)
(Test Circuit of Figure 2)



Provided in Figures 3, 4, and 6 are definitions of the switching intervals specified in the Electrical Characteristics. Figure 5 shows that the critical switching parameters stay under control at elevated temperatures.

In those applications where high voltage transients may occur while the output pin (Pin 4) is in the I_{sus} mode, excessive instantaneous power dissipation may occur, causing device failure. When this condition occurs, the control pin (Pin 2) can be used to shut off the output stage in order to protect the CS-287/8. As long as Pin 2 is in the high state (>1.5 volts, typ.), the output will remain off. One method of sensing the supply voltage and controlling Pin 2 is to use a resistor divider between the supply voltage and ground with Pin 2 connected to the resistor divider (see Fig. 1).

Another application option of the control pin is to use it to accomplish an enable/disable funtion. Since Pin 2 is compatible with TTL and CMOS logic levels, a logic low will enable the output, and allow it to follow the input signal at Pin 1. If Pin 2 is held at a logic high, the output will be disabled regardless of the state of the input signal.

If the control function is not being used in the application, it must be grounded or otherwise placed in a logic low state. If Pin 2 is left open, the output stage will remain off.

The output current in the I_{sus} mode should be oscillation free under most all operating conditions. There is a possibility that in a given application, the output current could oscillate for a small fraction of parts. If this was to occur, the remedy is place a capacitor from Pin 4 to Ground. The value of the capacitor should not exceed .01uF.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-287	TO-220
CS-288	TO-220

6

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-345A

IGNITION PRE-DRIVER

DESCRIPTION

The CS-345A is a monolithic integrated circuit which drives an external power transistor to start and regulate inductive load currents. A control input triggers the on-chip output transistor to saturate. An external resistor sets the CS-345A drive current up to 200mA. A sense input monitors the load current and triggers regulation at a user selectable level. Once the CS-345A begins regulating the load current, the status pin switches from a logic 1 to a logic 0. The control input switching to logic 0 causes the output transistor to go into cutoff, which shuts off the drive current to the load.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{DD}	-0.3	18	V
Differential Ground Voltage (Signal To Power GND)	V_{DGND}	-1	+1	V
Junction Temperature	T_J		150	°C
Operating Temperature	T_A	-40	105	°C
Storage Temperature	T_{STG}	-55	150	°C

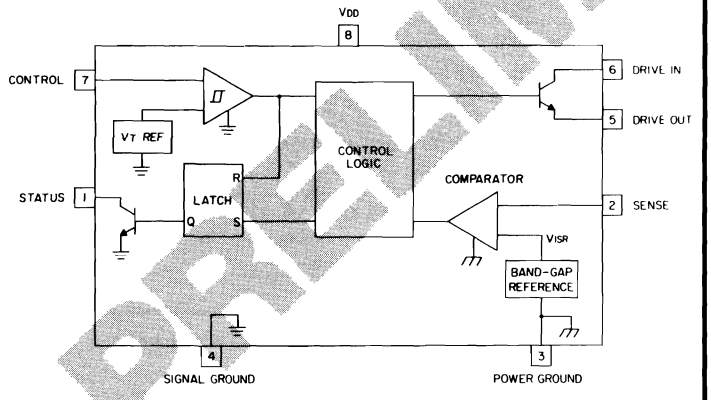
FEATURES:

- Trimmed internal voltage reference
- Total circuit delay, less than 10 μsec
- Maximum output transistor saturation voltage of 0.5V
- 200mA output drive current
- Available in 8 pin DIP

APPLICATIONS:

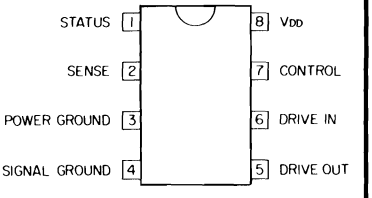
- Ignition Pre-Driver
- Motor Controller
- Solenoid Driver

BLOCK DIAGRAM



PIN CONNECTIONS

8L DIP



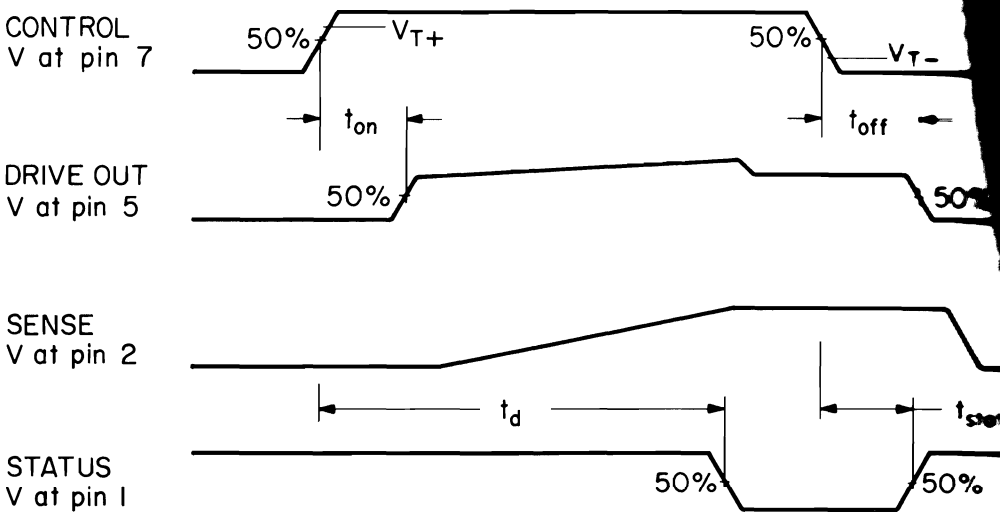
Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS (-40°C ≦ T_A ≦ 105°C, -40°C ≦ T_J ≦ 150°C, 7V ≦ V_{DD} ≦ 10V, all parameters are referenced to Power Ground unless otherwise noted)

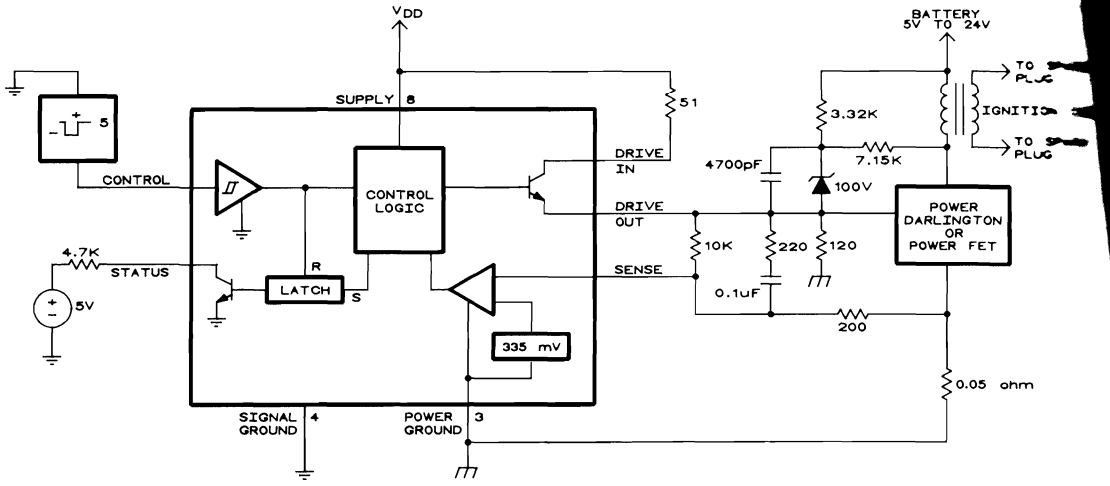
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply Voltage (referenced to "Ground")	V_{DD}		7	17	V
Supply Current Turn-on	$I+_{ON}$	Control high		25	mA
Supply Current Turn-off	$I+_{OFF}$	Control Low		5	mA
Differential Ground Current	I_{DGND}	V_{DGND} = -1V to +1V		20	mA
Control Input Threshold Voltage		(See Timing Diagram)			
Turn-on	V_T+	Control high		3.5	V
Turn-off	V_T-	Control low	0.9		V
Hysteresis ($V_T+ - V_T-$)	V_H		0.4	2.0	V
Control Input Leakage Current	I_{IL}	Control = 0V to 5.5V		±20	μA
Output Saturation Voltage ($V_{DRIVE\ IN} - V_{DRIVE\ OUT}$)	V_{SAT}	Control high $I_{DRIVE\ IN}$ = 200mA $V_{DRIVE\ OUT}$ = 0V to (V^+ - 4V) V_{DGND} = -1V to +1V		0.5	V
Input Leakage Current (at Drive In pin)	I_{IL}	Control low $V_{DRIVE\ IN}$ = V_{DD} $V_{DRIVE\ OUT}$ = -.3 to V_{DD} V_{DGND} = 0V		100	μA
Output Leakage Current (at Drive Out pin)	I_{OL}	Control low $V_{DRIVE\ IN}$ = V_{DD} $V_{DRIVE\ OUT}$ = -2 to 4V V_{DGND} = 0V		100	μA
Status Output Voltage "low"	V_{OL}	I_{STATUS} = 3mA V_{DGND} = 0V		0.4	V
Status Output Voltage "low"	V_{OL}	I_{STATUS} = 3mA V_{DGND} = -1V to +V		0.8	V
Status Output Leakage Current	I_{OL}	V_{STATUS} = 10V		10	μA
Drive Out Turn-on Delay From Control Turn-on	t_{on}	(See Timing Diagram)		30	μS
Drive Out Turn-off Delay From Control Turn-off	t_{off}	(See Timing Diagram)		10	μS
Status Turn-off Delay From Control Turn-off	t_{STATUS}	(See Timing Diagram)		30	μS
Status Disable Time	t_d	(See Timing Diagram)	150	600	μS
Sense Input Bias Current	I_{IB}	V_{SENSE} = -.3 to 0V V_{DGND} = -1V to +1V		10	μA
Sense Input Bias Current	I_{IB}	V_{SENSE} = 0 to +1V V_{DGND} = -1V to +1V		3	μA
Internal Sense Reference Voltage (includes input offset voltage)	V_{ISR}	V_{DGND} = -1V to +1V	315	355	mV
Supply Voltage Rejection Ratio	SVRR	f_{IN} = 5kHz to 20kHz V_{DD} = 7.1 to 9.9VDC V_{DD} (AC Component) = 0.2 to 2.0V_{p-p} V_{DGND} = 0V *NOTE: AC Component Should Not Cause V_{DD} to Go Below 7V or Above 17V.	45		dB

6

TIMING DIAGRAM



APPLICATION CIRCUIT



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-345A	8 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

CS-925

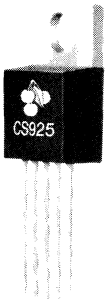
LOW DROPOUT REGULATOR
(WITH DELAYED RESET)

DESCRIPTION

The CS-925 is a low dropout, high current regulator. Included on-chip is a reset function with an externally set delay time. During power up, or after detection of any error in the regulated output, the reset pin will remain in the low state for the duration of the delay. Types of errors detected include short circuit, low input voltage, input transients, thermal shutdown, or others that cause the output to become unregulated. The current charging the delay capacitor (C3) is very low, thus allowing long delay times.

In automotive applications, the CS-925 and all regulated circuits are protected from reverse battery installations, as well as two-battery jumps. During line transients, such as a 60V load dump, the 0.75A regulator will automatically shut down to protect both internal circuits and the load.

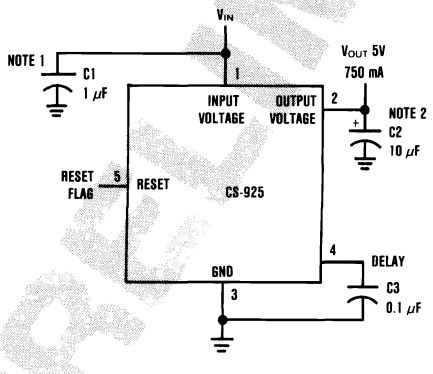
The CS-925 is packaged in a 5-lead TO-220, with copper tab for connection to a heat sink, if necessary.
NOTE: The CS-925 is pin compatible with the LM2925.



FEATURES:

- Input-output differential less than 0.6V at 0.5A
- Output current in excess of 750 mA
- Externally set delay for reset
- Reverse battery protection
- 60V load dump protection
- -50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Long delay times available

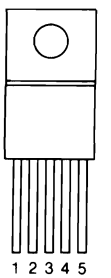
TEST AND APPLICATION CIRCUIT



NOTES:

1. C1 required if regulator is located far from power supply filter
2. C2 required for stability. . . value may be increased. Capacitor must be capable of operating at the minumum temperature expected.

PIN CONNECTIONS



TO-220
5-LEAD

1. Input voltage
2. Output voltage
3. Ground
4. Delay
5. Reset Output

6

ABSOLUTE MAXIMUM RATINGS

Input Voltage			
Operating Range	26V	Operating Temperature Range	−40°C to +125°C
Overvoltage Protection	60V	Maximum Junction Temperature	150°C
Internal Power Dissipation (Note 1)	Internally Limited	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS for V_{OUT} (V_{IN}=14V, C2 = 10 μf, I_O=500 mA, T_A=25°C (Note 2) unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	6V≤V_{IN}≤26V, I_O≤500 mA, −40°C≤T_j≤+125°C	4.80 4.75	5.00 5.00	5.20 5.25	V
Line Regulation	9V≤V_{IN}≤16V, I_O=5 mA 6V≤V_{IN}≤26V, I_O=5 mA		4 10	25 50	mV mV
Load Regulation	5 mA≤I_O≤500 mA		10	50*	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100Hz–10 kHz		200		mΩ
Quiescent Current	I_O≤10 mA I_O=500 mA I_O=750 mA		3 55 120	 100 	mA mA mA
Output Noise Voltage	10 Hz–100 kHz		100		μVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_O=120 Hz		66		dB
Dropout Voltage	I_O=500 mA I_O=750 mA		0.45 0.82	0.6 	V V
Current Limit		0.75	1.4		A
Maximum Operational Input Voltage		26	31		V
Maximum Line Transient	V_O≤5.5V	60	70		V
Reverse Polarity Input Voltage, DC	V_O≥−0.6V, 10Ω Load	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, -TA ≤ 100ms, 10Ω Load	−50	−80		V

*End of life limit is 65mV.

ELECTRICAL CHARACTERISTICS for Reset Output

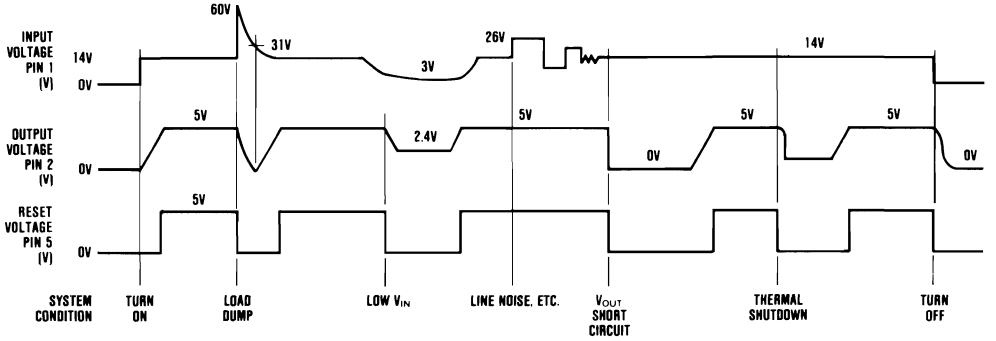
V_{IN}=14V, C_3 = 0.1μF, T_A=25°C (Note 2) (unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Voltage					
Output Low	I_{SINK} = 1.6 mA		0.3	0.6	V
Output High	I_{SOURCE} = 0	4.5	5.0	5.5	V
Reset Internal Pull-up Resistor			30		KΩ
Reset Output Current Limit	V_{RESET} = 1.2V		5		mA
V_{OUT} Threshold			4.5		V
Delay Time	C_3 = .005 μF C_3 = 0.1 μF C_3 = 4.7 μF tantalum		12 250 12		ms ms sec
Delay Current	Pin 4	1.2	1.6	2.0	μA

Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

Note 2: To ensure constant junction temperature, low duty cycle pulse testing is used.

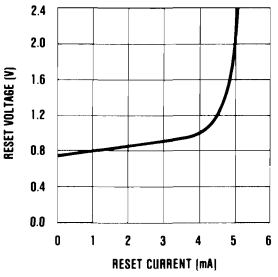
Typical Circuit Waveforms



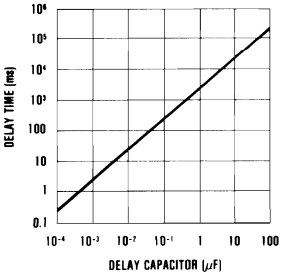
TL/H/5268-3

Typical Performance Characteristics

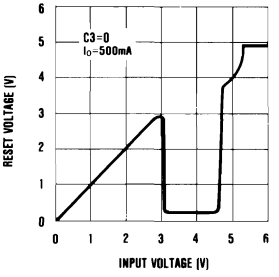
Reset Voltage



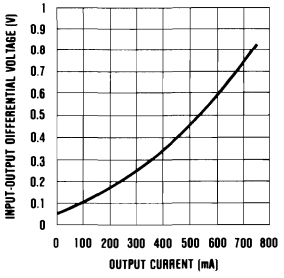
Delay Time



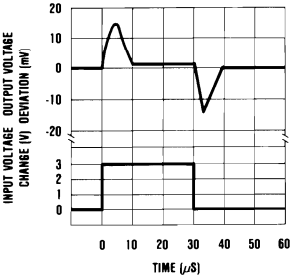
Reset Voltage on Power-up



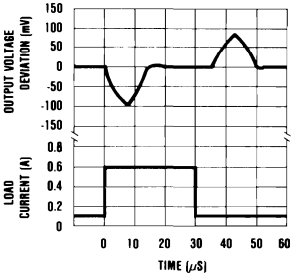
Dropout Voltage (V_{OUT})



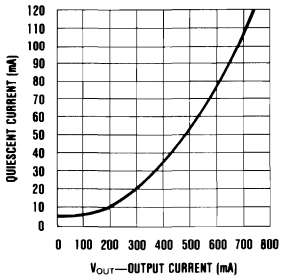
Line Transient Response



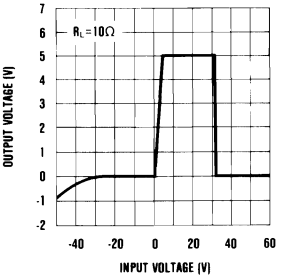
Load Transient Response



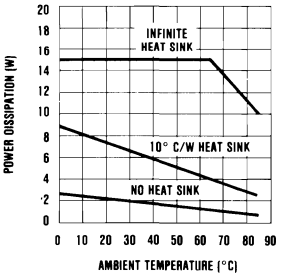
Quiescent Current



Output Voltage



Maximum Power Dissipation (TO-220)



6

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temeprature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Current Limit: Peak current that can be delivered to the output.

Application Hints

EXTERNAL CAPACITORS

The CS-925 output capacitor connected to pin 2 is required for stability. Without it, the regulator output will oscillate. The 10 μF shown is the minimum recommended value. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is usually determined at the minimum junction and ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to -40°C, capacitors rated at that temperature (such as tantalums) must be used.

RESET OUTPUT

The range of values for the delay capacitor is limited only by stray capacitances on the lower extreme and capacitance leakage on the other. Thus, delay times from microseconds to seconds are possible. The low charging current, typically 2.0 microamps, allows the use of small, inexpensive disc capacitors for the nominal range of 100 to 500 milliseconds. This is the time required in many microprocessor systems for the clock oscillator to stabilize when initially powered up. The RESET output of the regulator will thus prevent erroneous data and/or timing functions to occur during this part of operation. The same delay is incorporated after any other fault condition in the regulator output is corrected.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-925	TO220

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-935

LOW DROPOUT DUAL REGULATOR

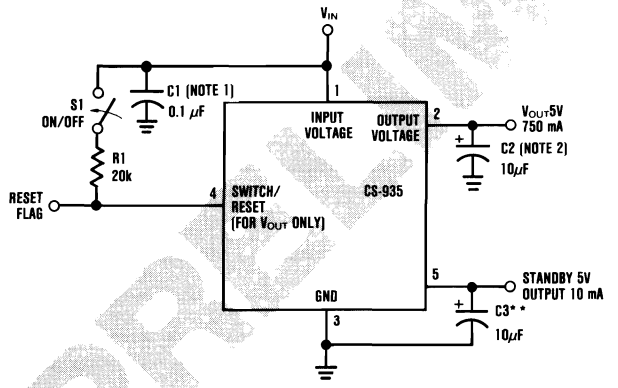
DESCRIPTION

The CS-935 is a low dropout, high current regulator. Also included is a standby 5V/10mA output for powering systems with standby memory. Quiescent current drain is less than 3mA when supplying 10mA loads from the standby regulator.

In automotive applications, the CS-935 and all regulated circuits are protected from reverse battery installations, as well as two-battery jumps. During line transients, such as a 60V load dump, the 0.75A regulator will automatically shut down to protect both internal circuits and the load, while the standby regulator will continue to power any standby load.

The CS-935 is packaged in a 5-lead TO-220, with copper tab for connection to a heat sink, if necessary.
NOTE: The CS-935 is pin-compatible with the LM2935.

TEST AND APPLICATION CIRCUIT



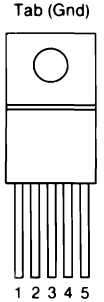
NOTES:

1. C1 required if regulator is located far from power supply filter.
2. C2 required for stability. . . value may be increased. Capacitor must operate at min. temp. expected.

FEATURES:

- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- -50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current output
- Reset error flag

PIN CONNECTIONS



1. Input voltage
2. Output voltage
3. Ground
4. Switch/reset
5. Standby/Output

6

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS for V_{OUT} (V_{IN}=14V, I_O=500 mA, T_j=25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	6V≤V_{IN}≤26V, I_O≤500 mA, -40°C≤T_j≤+125°C (Note 2)	4.75	5.00	5.25	V
Line Regulation	9V≤V_{IN}≤16V, I_O=5 mA 6V≤V_{IN}≤26V, I_O=5 mA		4 10	25 50	mV mV
Load Regulation	5 mA≤I_O≤500 mA		10	50*	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O≤10 mA, No Load on Standby I_O=500 mA, No Load on Standby I_O=750 mA, No Load on Standby		3 35 100	 100	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		μVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_O=120 Hz		66		dB
Dropout Voltage	I_O=500 mA I_O=750 mA		0.35 0.5	0.6	V V
Current Limit		0.75	1.4		A
Maximum Operational Input Voltage		26	31		V
Maximum Line Transient	V_O≤5.5V	60	90		V
Reverse Polarity Input Voltage, DC	V_O≥-0.6V, 10Ω Load	-15	-50		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ≤100ms, V_O≥-6V, 10Ω Load	-50	-80		V
Reset Output Voltage Low High	 R1=20k, V_{IN}=4.5V R1=20k, V_{IN}=14V	 4.5	 0.8 5.0	 1 5.5	 V V
Reset Output Current	V_{IN}=4.5V, Reset in Low State		5		mA
ON/OFF Resistor	R1 (⊥10% Tolerance)		20	30	kΩ

Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

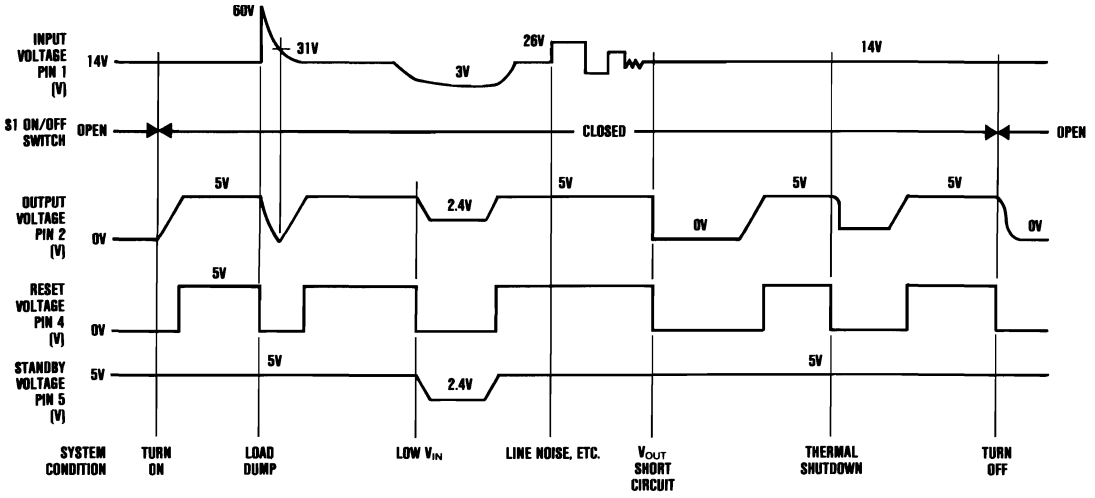
Note 2: The temperature extremes are guaranteed but not 100% production tested.

*End of life limit is 65mV.

ELECTRICAL CHARACTERISTICS FOR STANDBY OUTPUT (V_{IN}=14V, I_O=10 mA, T_j=25°C unless otherwise specified)

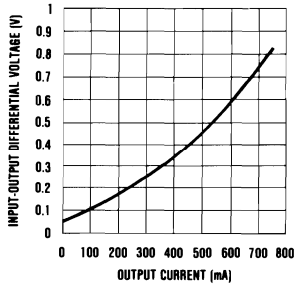
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$I_O \leq 10$ mA, $-40°C \leq T_j \leq 125°C$ $6V \leq V_{IN} \leq 26V$ (Note 2)	4.75	5.0	5.25	V
Tracking	V_{OUT}–Standby Output Voltage		50	200	mV
Line Regulation	$6V \leq V_{IN} \leq 26V$		4	50	mV
Load Regulation	$1\ mA \leq I_O \leq 10\ mA$		10	50	mV
Output Impedance	10 mA_{DC} and 1 mArms, 100 Hz-10 kHz		1		Ω
Quiescent Current	$I_O \leq 10$ mA, $-40°C \leq T_j \leq +125°C$, V_{OUT} OFF (Note 2)		2	3	mA
Output Noise Voltage	10 Hz-100 kHz		300		μV
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_o=120 Hz		66		dB
Dropout Voltage	$I_O \leq 10$ mA		0.3	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \leq V_O \leq 6V$	60	90		V
Reverse Polarity Input Voltage, DC	$V_O \leq -0.3V$, 510Ω Load	−15	−50		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, $\tau \leq 100$ ms, $V_O \geq -6V$ 500Ω Load	−50	−80		V

TYPICAL CIRCUIT WAVEFORMS

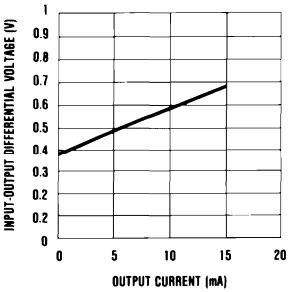


TYPICAL PERFORMANCE CHARACTERISTICS

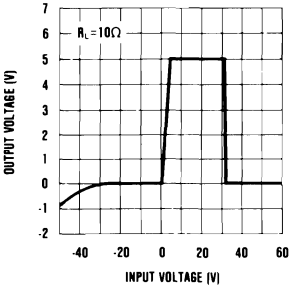
Dropout Voltage (V_{OUT})



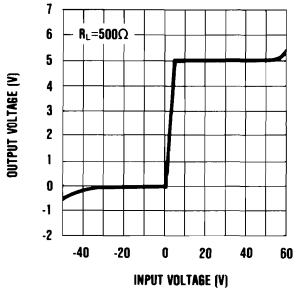
Dropout Voltage (V_{STBY})



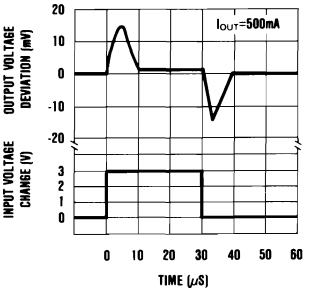
Output Voltage (V_{OUT})



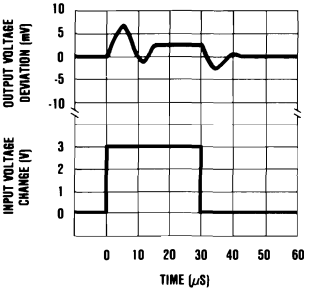
Output Voltage (V_{STBY})



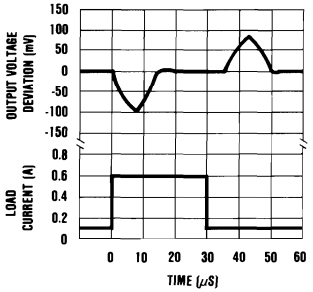
Line Transient Response (V_{OUT})



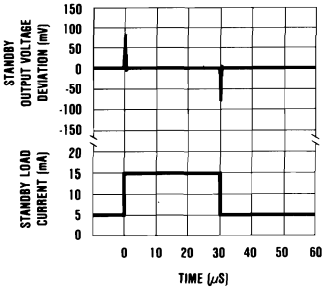
Line Transient Response (V_{STBY})



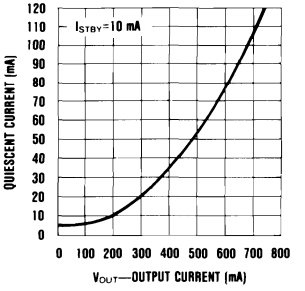
Load Transient Response (V_{OUT})



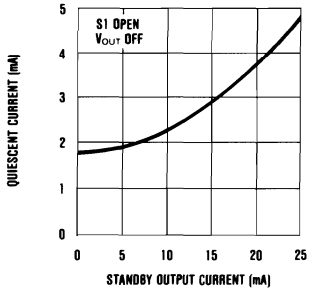
Load Transient Response (V_{STBY})



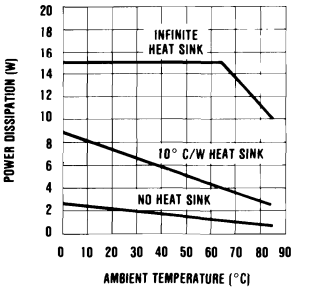
Quiescent Current (V_{OUT})



Quiescent Current (V_{STBY})



Maximum Power Dissipation (TO-220)



DEFINITION OF TERMS

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Current Limit: Peak current that can be delivered to the output

APPLICATIONS HINTS

EXTERNAL CAPACITORS

The CS-935 output capacitors are required for stability. Without them, the regulator outputs will oscillate. The 10μF shown are the minimum recommended values. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to - 40°C, capacitors rated at that temperature (such as tantalums) must be used.

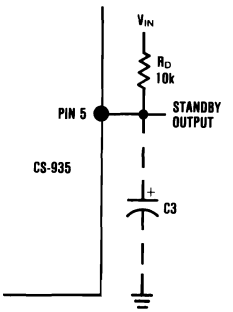
No capacitor should be attached to the ON/OFF and RESET FLAG pin. Due to the internal circuits of the IC, oscillation on this pin could result.

STANDBY OUTPUT

The CS-935 differs from most fixed voltage-regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator ouput can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 5.7V zener, the current through the external resistor should be sufficient to bias Pin 5 up to this point. Approximately 60μA will suffice, resulting in a 10k external resistor for most applications.



Disabling Standby Output to Eliminate C3

HIGH CURRENT OUTPUT

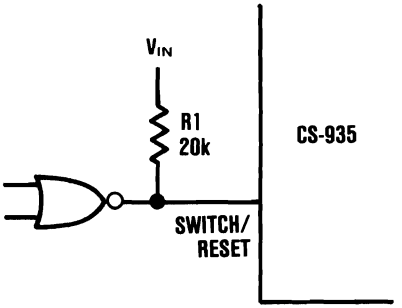
Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

ON/OFF AND RESET FLAG PIN

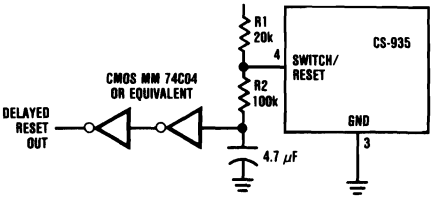
This pin has the ability to serve a dual purpose if desired. When controlled in the manner shown in the test circuit (common in automotive systems where S1 is the ignition switch), the pin also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. In other words, under normal operating conditions, the output voltage of this pin is high (5V). This is set by an internal clamp. If the high current output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the pin switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

Application Hints (Continued)

The ON/OFF pin can also be driven directly from logic circuits. The only requirement is that the 20k pull-up resistor remain in place. This will not affect the logic gate since the voltage on this pin is limited by the internal clamp to 5V. The error flag is sacrificed in this arrangement since the maximum sink capability of the pin in the active low state approximately 5 mA) is usually not sufficient to pull down the active high logic gate. Of course, the flag can be retained if the driving gate is open collector logic.



Controlling ON/OFF Terminal with a Typical CMOS or TTL Logic Gate



Reset Pulse on Power-Up (with approximately 300 ms delay)

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-935	TO220

CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CSC™ CHERRY SEMICONDUCTOR

CS-945

LOW DROPOUT DUAL REGULATOR

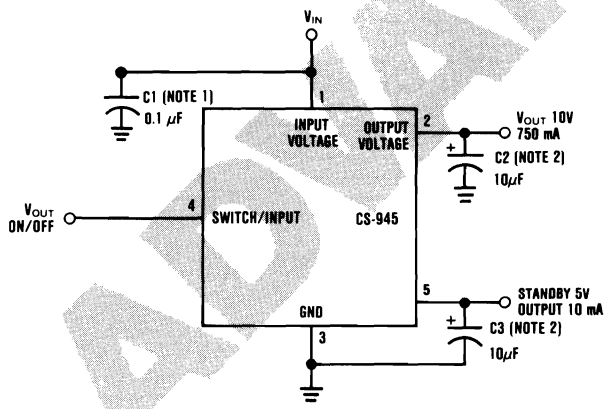
DESCRIPTION

The CS-945 is a low dropout, high current regulator. Also included is a standby 5V/10mA output for powering systems with standby memory. Quiescent current drain is less than 3mA when supplying 10mA loads from the standby regulator.

In automotive applications, the CS-945 and all regulated circuits are protected from reverse battery installations, as well as two-battery jumps. During line transients, such as a 60V load dump, the 0.75A regulator will automatically shut down to protect both internal circuits and the load, while the standby regulator will continue to power any standby load.

The CS-945 is packaged in a 5-lead TO-220, with copper tab for connection to a heat sink, if necessary.

TEST AND APPLICATION CIRCUIT



NOTES:

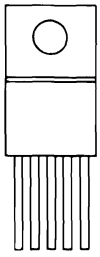
1. C1 required if regulator is located far from power supply filter.
2. Required for stability. . . value may be increased. Capacitor must operate at min. temp. expected.

FEATURES:

- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- -50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current output

PIN CONNECTIONS

Tab (Gnd)



1. Input voltage
2. Output voltage
3. Ground
4. Switch Input
5. Standby Output

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 3)	Internally Limited
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS for V_{OUT} (V_{IN}=14V, I_O=500 mA, T_j=25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	11V≤V_{IN}≤26V, I_O≤500 mA, -40°C≤T_j≤+125°C (Note 4)	9.4	10	10.6	V
Line Regulation	11V≤V_{IN}≤16V, I_O=5 mA 11V≤V_{IN}≤26V, I_O=5 mA		8 20	40 80	mV mV
Load Regulation	5 mA≤I_O≤500 mA			50*	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O≤10 mA, No Load on Standby I_O=500 mA, No Load on Standby I_O=750 mA, No Load on Standby			7 120 250	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100	500	μVrms
Long Term Stability			50		mV/1000 hr
Ripple Rejection	f_O=120 Hz		53		dB
Dropout Voltage	I_O=500 mA			0.6	V
Current Limit		0.75	1.4	2.5	A
Maximum Operational Input Voltage		26	31	36	V
Maximum Line Transient	V_O≤11V	60			V
Reverse Polarity Input Voltage, DC	V_O≥-0.6V, 10Ω Load	-18			V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ≤100ms, V_O≥-6V, 10Ω Load	-50			V
Input Switch Threshold	V_{OUT} Off			0.8	V
	V_{OUT} On	2.0			
Input Switch Current	Input Voltage Range 0 to 26V	-10		10	uA

Note 3: Thermal resistance without a heat sink for junction to case temperature is 4°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

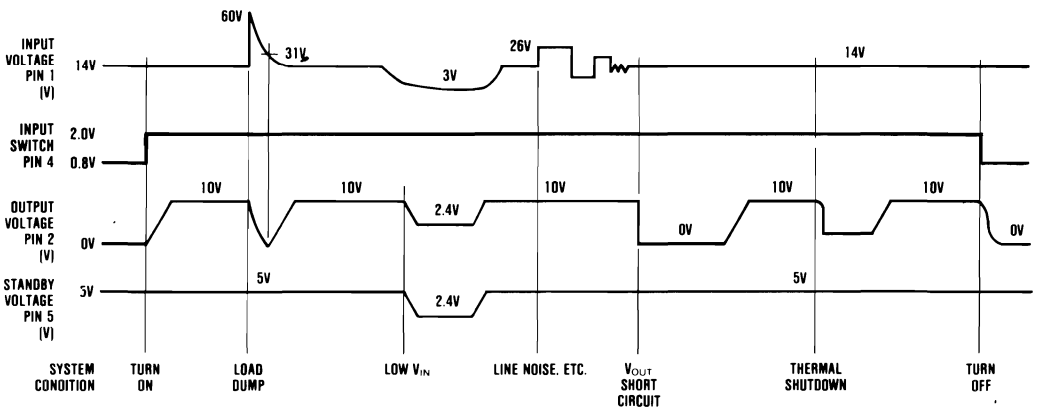
Note 4: The temperature extremes are guaranteed but not 100% production tested.

*End of life limit is 65mV.

ELECTRICAL CHARACTERISTICS FOR STANDBY OUTPUT (V_{IN}=14V, I_O=10 mA, T_j=25°C unless otherwise specified)

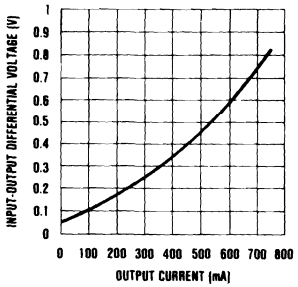
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$I_O \leq 10$ mA, $-40°C \leq T_j \leq 125°C$ $6V \leq V_{IN} \leq 26V$ (Note 4)	4.75	5.0	5.25	V
Line Regulation	$6V \leq V_{IN} \leq 26V$		4	50	mV
Load Regulation	$1\ mA \leq I_O \leq 10\ mA$		10	50	mV
Output Impedance	10 mA_{DC} and 1 mArms, 100 Hz-10 kHz		1		Ω
Quiescent Current	$I_O \leq 10$ mA, $-40°C \leq T_j \leq +125°C$, V_{OUT} OFF (Note 4)		2	3	mA
Output Noise Voltage	10 Hz-100 kHz		300		μV
Long Term Stability			50		mV/1000 hr
Ripple Rejection	f_o=120 Hz		66		dB
Dropout Voltage	$I_O \leq 10$ mA		0.55	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \leq V_O \leq 6V$	60			V
Reverse Polarity Input Voltage, DC	$V_O \leq -0.3V$, 510Ω Load	-18			V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, $\tau \leq 100$ ms, $V_O \geq -6V$ 500Ω Load	-50			V

TYPICAL CIRCUIT WAVEFORMS

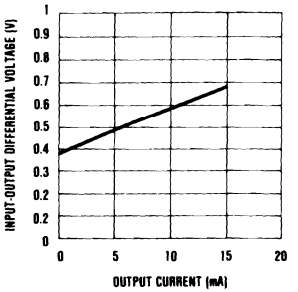


TYPICAL PERFORMANCE CHARACTERISTICS

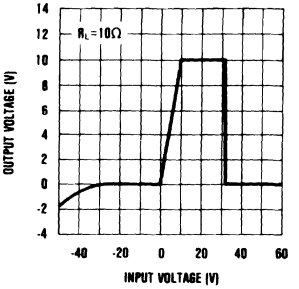
Dropout Voltage (V_{OUT})



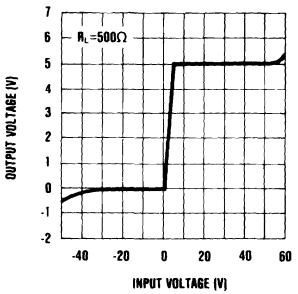
Dropout Voltage (V_{STBY})



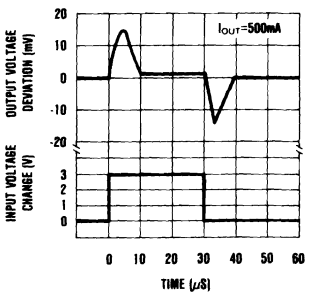
Output Voltage (V_{OUT})



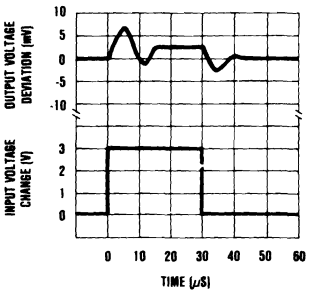
Output Voltage (V_{STBY})



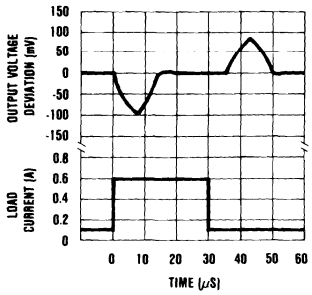
Line Transient Response (V_{OUT})



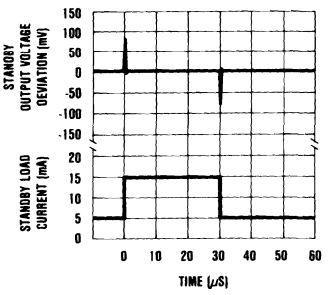
Line Transient Response (V_{STBY})



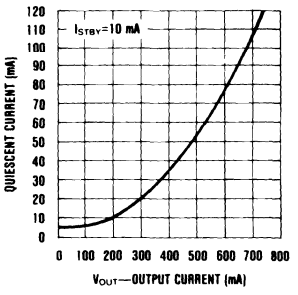
Load Transient Response (V_{OUT})



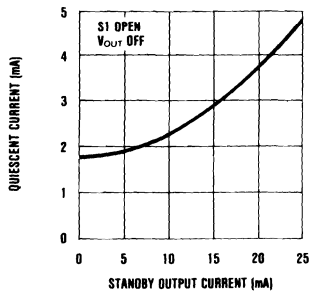
Load Transient Response (V_{STBY})



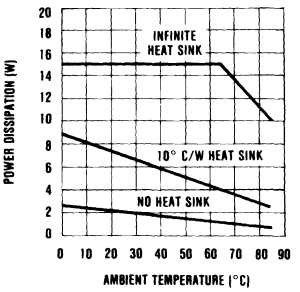
Quiescent Current (V_{OUT})



Quiescent Current (V_{STBY})



Maximum Power Dissipation (TO-220)



DEFINITION OF TERMS

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Current Limit: Peak current that can be delivered to the output

APPLICATIONS HINTS

EXTERNAL CAPACITORS

The CS-945 output capacitors are required for stability. Without them, the regulator outputs will oscillate. The 10μF shown are the minimum recommended values. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

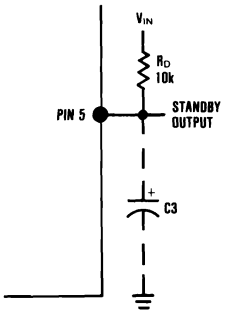
Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to - 40°C, capacitors rated at that temperature must be used.

STANDBY OUTPUT

The CS-945 differs from most fixed voltage-regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator ouput can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 6.0V zener, the current through the external resistor should be sufficient to bias Pin 5 up to this point. Approximately 60μA will suffice, resulting in a 10k external resistor for most applications.



Disabling Standby Output to Eliminate C3

HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-945	TO-220

CSC™ CHERRY SEMICONDUCTOR

CS-955

LOW DROPOUT DUAL REGULATOR

DESCRIPTION

The CS-955 is a low dropout, high current regulator. Also included is a standby 5V/20mA output for powering systems with standby memory. Quiescent current drain is less than 3mA when supplying 10mA loads from the standby regulator

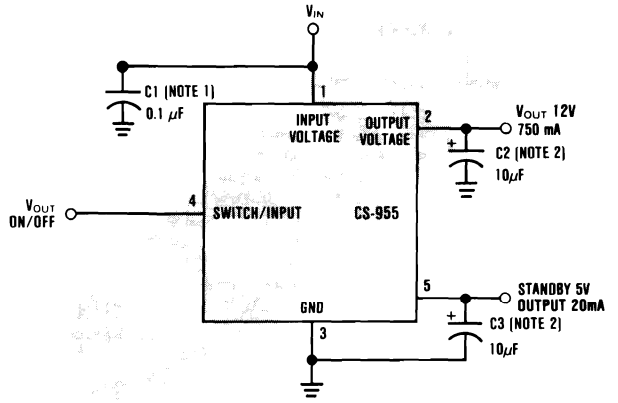
In automotive applications, the CS-955 and all regulated circuits are protected from reverse battery installations, as well as two-battery jumps. During line transients, such as a 60V load dump, the 0.75A regulator will automatically shut down to protect both internal circuits and the load, while the standby regulator will continue to power any standby load.

The CS-955 is packaged in a 5-lead TO-220, with copper tab for connection to a heat sink, if necessary.

FEATURES:

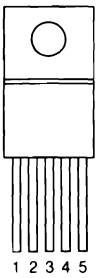
- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- -50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current output

TEST AND APPLICATION CIRCUIT



PIN CONNECTIONS

Tab (Gnd)



1. Input voltage
2. Output voltage
3. Ground
4. Switch Input
5. Standby Output

NOTES:

1 C1 required if regulator is located far from power supply filter

2. Required for stability. . . value may be increased. Capacitor must operate at min. temp. expected.

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 3)	Internally Limited
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS for V_{OUT} (V_{IN}=14V, I_O=500 mA, T_j=25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	13V≤V_{IN}≤26V, I_O≤500 mA, -40°C≤T_j≤+125°C (Note 4)	11.4	12	12.6	V
Line Regulation	13V≤V_{IN}≤26V, I_O=5 mA		15	80	mV
Load Regulation	5 mA≤I_O≤500 mA			50	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O≤10 mA, No Load on Standby I_O=500 mA, No Load on Standby I_O=750 mA, No Load on Standby		3 40 90	7 100	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		μVrms
Long Term Stability			50		mV/1000 hr
Ripple Rejection	f_O=120 Hz		53		dB
Dropout Voltage	I_O=500 mA			0.6	V
Current Limit		0.75	1.4	2.5	A
Maximum Operational Input Voltage		26	31	36	V
Maximum Line Transient	V_O≤13V	60			V
Reverse Polarity Input Voltage, DC	V_O≥-0.6V, 10Ω Load	-18	-30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ≤100ms, V_O≥-6V, 10Ω Load	-50	-80		V
Input Switch Threshold	V_{OUT} Off		1.25	0.8	V
	V_{OUT} On	2.0	1.25		
Input Switch Current	Input Voltage Range 0 to 26V	-10		10	uA

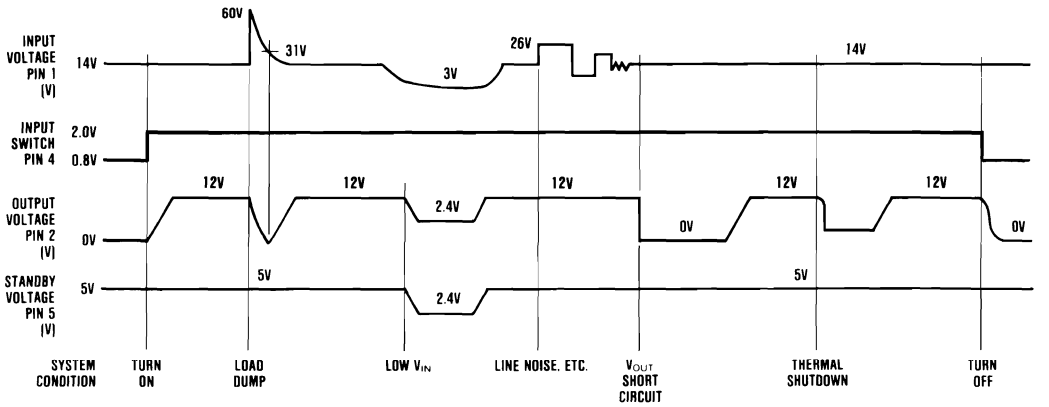
Note 3: Thermal resistance without a heat sink for junction to case temperature is 4°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

Note 4: The temperature extremes are guaranteed but not 100% production tested.

ELECTRICAL CHARACTERISTICS FOR STANDBY OUTPUT (V_{IN}=14V, I_O=10 mA, T_j=25°C unless otherwise specified)

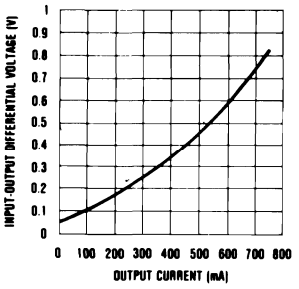
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$I_O \leq 10$ mA, $-40°C \leq T_j \leq 125°C$ $6V \leq V_{IN} \leq 26V$ (Note 4)	4.75	5.0	5.25	V
Line Regulation	$6V \leq V_{IN} \leq 26V$		4	50	mV
Load Regulation	$1\ mA \leq I_O \leq 10\ mA$		10	50	mV
Output Impedance	10 mA_{DC} and 1 mArms, 100 Hz-10 kHz		1		Ω
Quiescent Current	$I_O \leq 10$ mA, $-40°C \leq T_j \leq +125°C$, V_{OUT} OFF (Note 4)		2	3	mA
Output Noise Voltage	10 Hz-100 kHz		300		μV
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_o=120 Hz		66		dB
Dropout Voltage	$I_O \leq 10$ mA		0.55	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \leq V_O \leq 6V$	60			V
Reverse Polarity Input Voltage, DC	$V_O \leq -0.3V$, 510Ω Load	-18	-30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, $\tau \leq 100$ ms, $V_O \geq -6V$ 500Ω Load	-50	-80		V

TYPICAL CIRCUIT WAVEFORMS

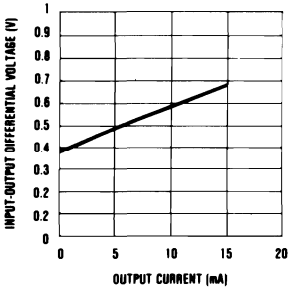


TYPICAL PERFORMANCE CHARACTERISTICS

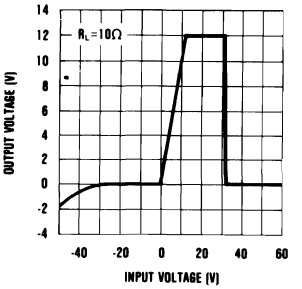
Dropout Voltage (V_{OUT})



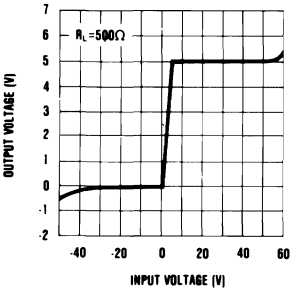
Dropout Voltage (V_{STBY})



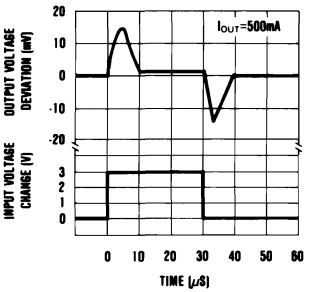
Output Voltage (V_{OUT})



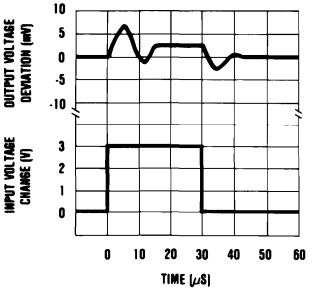
Output Voltage (V_{STBY})



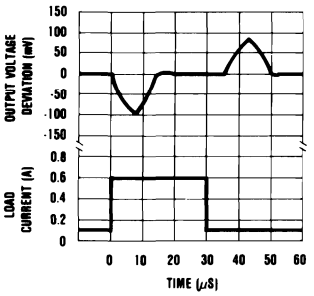
Line Transient Response (V_{OUT})



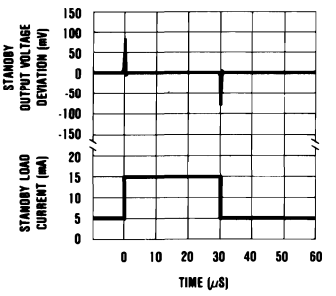
Line Transient Response (V_{STBY})



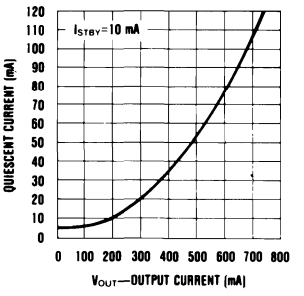
Load Transient Response (V_{OUT})



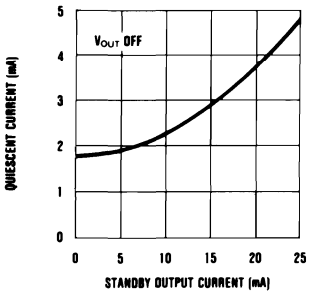
Load Transient Response (V_{STBY})



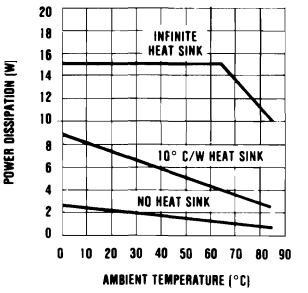
Quiescent Current (V_{OUT})



Quiescent Current (V_{STBY})



Maximum Power Dissipation (TO-220)



6

DEFINITION OF TERMS

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Current Limit: Peak current that can be delivered to the output

APPLICATIONS HINTS

EXTERNAL CAPACITORS

The CS-955 output capacitors are required for stability. Without them, the regulator outputs will oscillate. The 10μF shown are the minimum recommended values. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

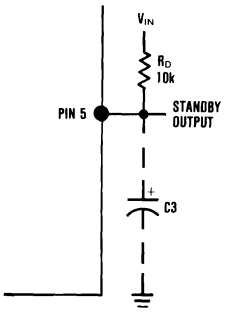
Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to - 40°C, capacitors rated at that temperature must be used.

STANDBY OUTPUT

The CS-955 differs from most fixed voltage-regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator ouput can be controlled with the ON/OFF pin, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 6.0V zener, the current through the external resistor should be sufficient to bias Pin 5 up to this point. Approximately 60μA will suffice, resulting in a 10k external resistor for most applications.



Disabling Standby Output to Eliminate C3

HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-955	TO-220

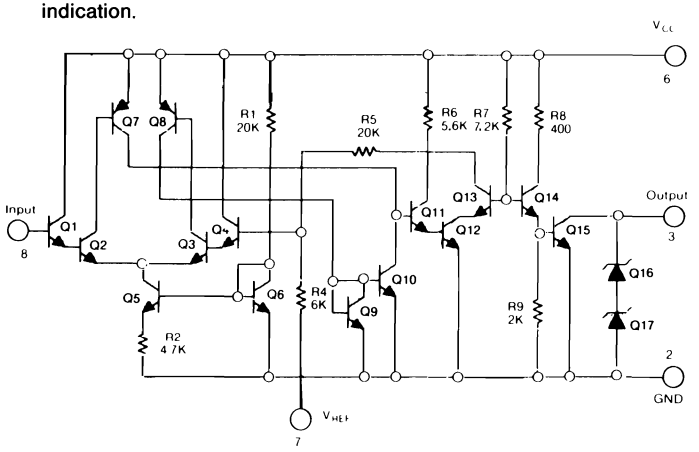
CSC™ CHERRY SEMICONDUCTOR

CS-102-1
CS-102-2

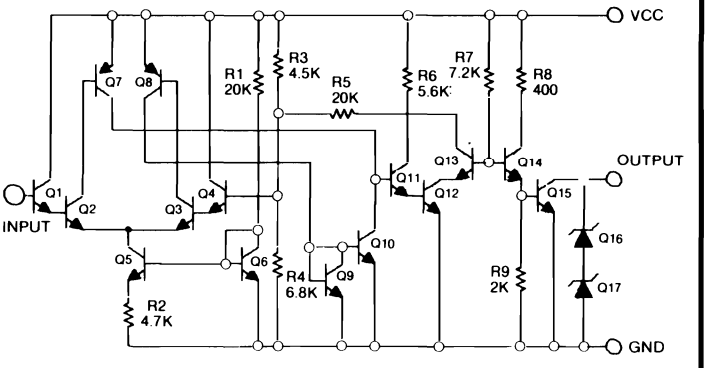
LEVEL DETECTING ICs with SCHMITT TRIGGERS

DESCRIPTION

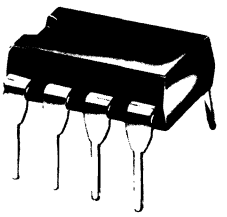
The CS-102-1 and CS-102-2 are monolithic integrated circuit level detectors with controlled hysteresis and are designed for applications requiring the function of a Schmitt trigger along with superior voltage and temperature stability. With input sensitivity below 35 namoamperes these ICs are ideally suited for use with high impedance resistance dividers or voltage inputs as well as level detection of approximately one time constant in R-C timing applications. (CS-102-2 also has an internal reference of 0.6 of the supply voltage.) The output is zener diode clamped for driving inductive loads and it can sink up to 70mA of current. These devices are particularly suited for battery powered applcation and low-light indication.



SCHEMATIC DIAGRAM — CS-102-1

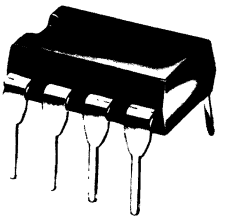


SCHEMATIC DIAGRAM — CS-102-2



TERMINAL ASSIGNMENTS CS-102-1

PIN 1 — N.C.	PIN 5 — N.C.
PIN 2 — GND	PIN 6 — V_{CC}
PIN 3 — OUTPUT	PIN 7 — V_{REF}
PIN 4 — N.C.	PIN 8 — INPUT



TERMINAL ASSIGNMENTS CS-102-2

PIN 1 — N.C.	PIN 5 — N.C.
PIN 2 — GND	PIN 6 — V_{CC}
PIN 3 — OUTPUT	PIN 7 — INPUT
PIN 4 — N.C.	PIN 8 — N.C.

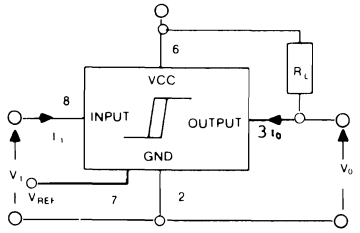
ABSOLUTE MAXIMUM RATINGS

CS-102-1 & CS-102-2

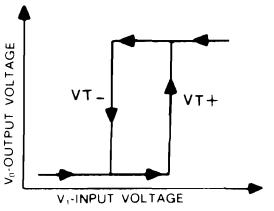
Power Supply Voltage	V_{CC}	9.0V
Output Current	I_O	150mA
Input Voltage	V_I	V_{CC}
Output Voltage	V_O	12V
Storage Temperature	T_S	-40°C to 150°C
Operating Temperature	T_A	-20°C to 70°C

7

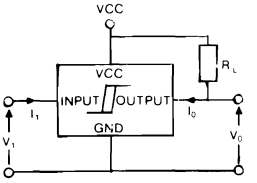
Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157



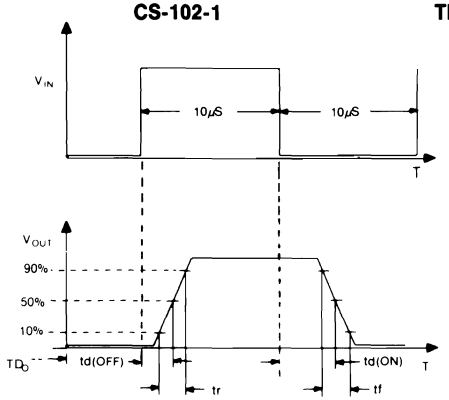
TEST CIRCUIT
CS-102-1



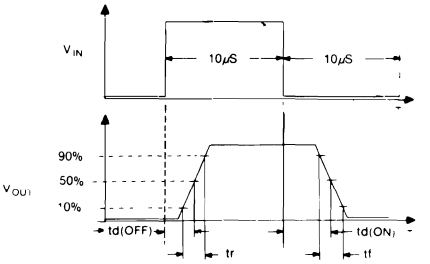
TRANSFER CHARACTERISTICS
CS-102-1 & CS-102-2



TEST CIRCUIT
CS-102-2



SWITCHING WAVEFORMS CS-102-1



SWITCHING WAVEFORMS CS-102-2

ELECTRICAL CHARACTERISTIC: V_{CC} = 2.7V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS-102-1 and CS-102-2						
I_I	Input Current	$V_I = V_T + (T_a$ = 25°C to 70°C)		5	35	nA
VO (on)	On-state output voltage	V_I = 0 I_O = 70mA		0.25	0.50	V
IO (off)	Off-state output current (leakage)	V_I = 2.7V V_O = 2.7V		0.001	1.0	μA
VZ	Zener breakdown voltage	I_O = 12mA	11	15	19	V
I_{CC} (off)	Supply Current, output off	V_I = 2.7V R_L 0		1	2.5	mA
I_{CC} (on)	Supply Current, output on	V_I = 0 R_L = 0		4	10	mA
V_T	Threshold voltage variation over supply and operating temperature			±2	±5	%
tr, tf	Switching times, rise and fall	R_L = 33Ω		0.5		μS
t_d(on),t_d(off)	Propagation delay	R_L = 33Ω		2.0		μS
CS-102-2						
VT +	Positive-going threshold voltage		1.43	1.62	1.78	V
VT −	Negative-going threshold voltage		1.30	1.43	1.57	V
VT +/V_{CC}	Ratio of positive-going threshold voltage to supply voltage	V_{CC} = 2.0 to 9.0V	0.54	0.60	0.66	—
VT −/V_{CC}	Ratio of negative-going threshold voltage to supply voltage	V_{CC} = 2.0V to 9.0V	0.48	0.53	0.58	—

ORDERING INFORMATION

Part Number	Description
CS-102-1	8 lead PDIP
CS-102-2	8 lead PDIP

CSC™ CHERRY SEMICONDUCTOR

CS-209

PROXIMITY DETECTOR

ELECTRO-MAGNETIC PROXIMITY SENSING ICs

DESCRIPTION

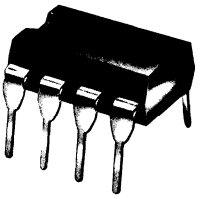
The CS-209 is a Bipolar Monolithic Integrated Circuit for Proximity sensing applications. The circuit contains an on-chip regulated supply, oscillator, demodulator, level detector, and output stages.

The Oscillator, together with an external LC network, provides controlled oscillations where the amplitude is highly dependant on the Q of the LC network. During low Q conditions, a variable low level feedback is applied to maintain oscillation. The peak demodulator detects the negative portion of the oscillator envelope and the demodulated waveform is then compared to an internal reference by the level detector.

The CS-209 has two high level outputs with external loads.

The current sink circuit provides a constant discharge current at the input of the amplifier.

The CS-209 contains transient supression circuits which absorb negative transients at the tank circuit terminal.



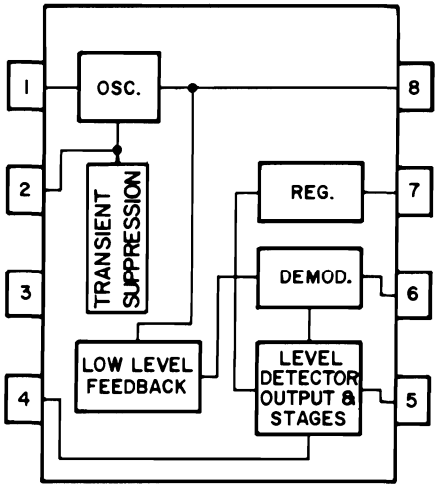
FEATURES:

- Regulated Supply
- Negative Transient Suppression
- Variable Low Level Feedback

APPLICATIONS:

- Ignitions
- Coin Sensors
- Metal Detectors
- Proximity Switches

BLOCK DIAGRAM



7

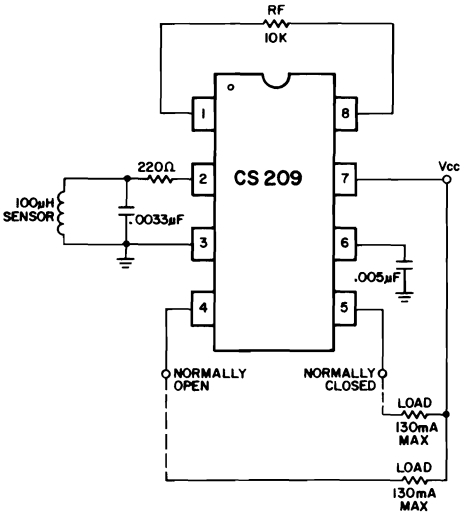
Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 24V
Power Dissipation (T_A = 125°C) 200mW
Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... 150°C

SPECIFICATIONS (T_A = 25°C and V_{cc} = 20V unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage V_7/V_{12}		4		24	V
Supply Current I_7/I_{12}	V_{cc} = 4.0V		4.5	6	mA
Output Saturation Voltage:					
CS-209 V_4	I_4 = 124 mA		0.2	0.5	V
CS-209 V_5 V_6	I_5 = 124 mA		0.2	0.5	V
Charge Current	I_6	20	30	40	μA
Leakage Current:					
CS-209 I_4	V_4 = 24 mA			100	μA
CS-209 I_5	V_5 = 24V			100	μA



PROXIMITY SWITCH

ORDERING INFORMATION

PART NUMBER	PACKAGE
CS-209	8 LEAD PDIP

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-212

SECURITY DETECTOR
DATA RECEIVER/TRANSMITTER

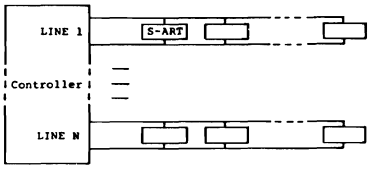
SERIAL-ADDRESSABLE RECEIVER/TRANSMITTER

INTRODUCTION

The S-ART is a 16 pin circuit designed for data transmission on a two-lead cable. The circuit is specially developed for alarm systems where it is desired to identify each detector individually. There can be up to 30 S-ART circuits/detectors on the same 2-lead cable. This cable transmits both DC supply to the S-ART and information to/from the S-ART

SYSTEM BLOCK DIAGRAM

A method by which, in principle, the system can be extended to an infinite number of S-ART is shown on the block diagram. The controller scans the in/outputs of a number of lines, each with a maximum of 30 S-ARTs.



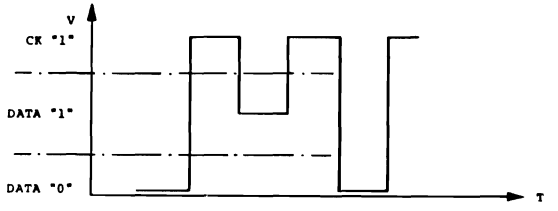
DESCRIPTION

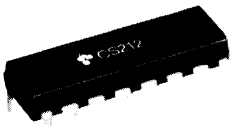
The S-ART works on the principle by which an address is sent on the line cable and the S-ART which recognizes the address then carries out the order which can, in principle, be two things:

1. Transmit data from the line cable to the S-ART's two outputs OUT 0 and OUT 1
2. Answer the S-ART controller with the condition of the 2 inputs IN 0 and IN 1/IN 2-3.

The line signal is divided into 3 levels in order to give a time signal for synchronizing and a data signal containing addresses, orders etc.

Typical signal levels for the three levels would be 15V, 7.5V and 0V





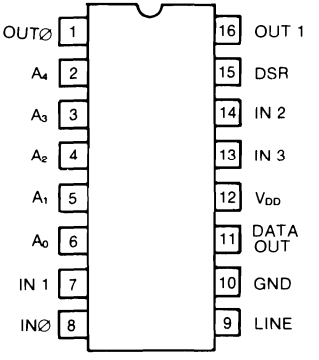
FEATURES:

- Receives/transmits data on only two leads
- Low current consumption
- High noise immunity
- Sabotage surveilled loop input

APPLICATIONS:

- Security systems
- Fire detection
- Surveillance
- Building automation
- Local data transmission

PIN CONNECTIONS



(Top View)

7

SPECIFICATIONS

ADDRESS CODING

The circuit is coded on address inputs A0-A4.

In order to reduce the power consumption to the circuits they are in power down mode for most of the time. Only when a circuit is addressed is the amount to that particular circuit increased.

READ

When a S-ART has recognized an address with the correct parity and then received a READ-order the controller becomes passive. The S-ART in question will then send data bits to the controller. These bits are the condition on the IN 0 and IN 1/IN 2-3 and a parity bit derived from them.

The current in inputs IN 0 and IN 1 only flows when the S-ART is addressed.

If the sabotage surveilled loop IN 2-3 is used IN 1 should be open. IN 2-3 is then read instead of IN 1.

The loop IN 2-3 is checked for both shorting and breaking.

WRITE

When a S-ART has recognized an address with correct parity and a write order, the S-ART in question transmits data to the utputs OUT 0 and OUT 1. This data transmission takes place after a check of the parity bit. It the parity bit is wrong, data transmission to OUT 0 and OUT 1 is blocked and new data transmission can only take place after a read order which resets the parity fault.

The DSR signal can be used to strobe OUT 0 and OUT 1 further on in the following logic.

CHARACTERISTICS	CONDITIONS	LIMITS +25° C MIN.	LIMITS +25° C TYP.	LIMITS +25° C MAX.	UNITS
Device Current I_{dd} Not Addressed	Outputs unloaded Line Voltage=0-15V V_{dd}=15V		.47	0.80	mA
Device Current I_{dd} Power-Up Mode (5 corr. addr. bits) C_p4-C_p5	IN0, IN1 are open IN2, IN3 are active V_{dd}=15V		3.55	5.50	mA
Device Current I_{dd} Addressed, Line Output Transistor Active	IN2, IN3 not active IN0, IN1 are open V_{dd}=15V		6.24	9.64	mA
Device Current I_{dd} Addressed (4 corr. addr. bits) Line Output Transistor Not Active	IN2, IN3 not active IN0, IN1 are open V_{dd}=15V		1.84	2.86	mA
Output Voltage Low Level Out 0, Out 1, DSR	Vdd=10-15V I_{sink}=1mA			1.2	V
Output sink Current Out 0, Out 1, DSR		1.0			mA
Output Voltage High Level Out 0, Out 1, DSR				14	V
Leakage Current Out 0, Out 1, DSR	V_{out}=14V			30	μA
Input Voltage Level Low	V_{dd}=10-15V			30%V_{dd}	V
A0-A4, IN0, IN1 High	V_{dd}=10-15V	70%V_{dd}			V
Input Current IN0, IN1=GND Power-Up Mode (4 corr. addr. bits)	V_{dd}=18V	150		850	μA
Input Current A0-A4, IN0, IN1 Not Addressed	V_{dd}=18V			20	μA
Positive Trigger Threshold V_p, C	Clock Comparator	11.0	11.7	12.4	V
Voltage V_{dd}=15V V_p, D	Data Comparator	4.6	5.7	6.6	V
Negative Trigger V_{nc}	V_{dd}=15V Clock Comparator	10.2	10.9	11.6	V
Threshold Voltage V_{nc}	V_{dd}=15V Data Comparator	3.4	4.3	5.2	V
Hysteresis Voltage Clock/Data Comp.	V_{dd}=15V	0.7	0.8		V
Saturation Voltage For Line Output Driver	V_{dd}=15V I_c=50 mA			1	V
Saturation Voltage For Line Output Driver	V_{dd}=15V I_c=10 mA			0.4	V
Leakage Current For the Line Output	V_{line}=0-18V V_{dd}=18V			±16	μA
Line Signal Freq.	V_{dd}=15V±1V	0		20	kHz
Rise/Fall-Time Line Signal		0.250		250	μS
Turn-On Time for Line Output Driver			1.0		μS
Turn-Off Time for Line Output Driver			1.0		μS
•Line Voltage VL		0		28	V
Loop Current IN2, IN3		0.1		0.5	mA
Alarm Condition IN2-IN3 Loop Open		1		5	kΩ
Alarm Condition IN2-IN3 Loop Shorted		5		30	kΩ
Temperature T_A	Operating	-40		85	°C
Range T_{stg}	Storage	-65		150	°C

•The circuit shall function in the correct way only between 0-18V. Data driver must not turn on when line voltage is above 18V.

DATA FORMAT

The signals are sent out on the line in words organized as shown in the figure.

The S-ART information consists of two parity bits - an address parity bit and a data parity bit. Both the address and data are checked for even parity. The address parity bit must always be generated by the controller. The data parity bit during the READ-mode is generated by the S-ART. During the WRITE-mode the data parity bit is generated by the controller.

A0-A4:
Address inputs. Must be connected to V_{DD} or GND according to the relevant address code.

LINE:
Signal lead in the line cable.

GND:
Zero lead in the line cable.

V_{DD}:
Supply voltage to the S-ART. The voltage is derived from the line signal.

IN 0:
Input to S-ART

IN 1:
Input to S-ART

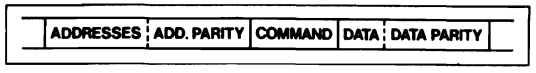
IN 2—IN 3:
Sabotage surveilled loop (shorting and breaking).

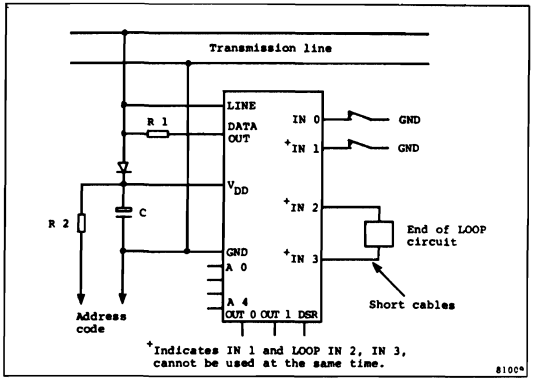
OUT 0:
Output (open collector) from S-ART

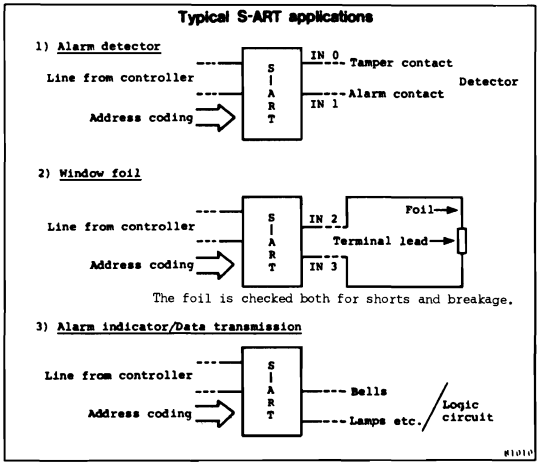
OUT 1:
Output (open collector) from S-ART

DSR:
Data set ready. Output (open collector) from the S-ART, which is active during WRITE-mode, when OUT 0 and OUT 1 change.

DATA OUT:
Output from the S-ART, which is active in the READ-mode. Transmits data from S-ART to line.







CS-212 FUNCTIONAL DESCRIPTION

7

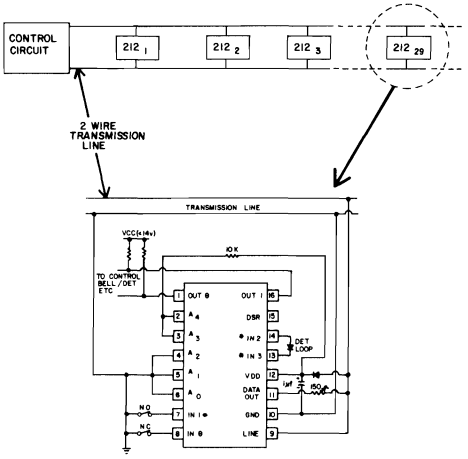
GENERAL

The CS-212 is a peripheral addressable circuit which is used as a communication link between Dectectors/Sensors and a Central Control Unit.

The communication between the CS-212 and a control unit takes place via a simple 2-wire cable which also provides power to the IC.

On each 2-wire cable, a maximum of 30 CS-212's can be controlled or interrogated with the address binary 0-29. This permits surveillance of up to 30 window protections, door contacts, movement detectors, etc., within the same 2-wire group. Each 212 can monitor the status of two external surveillance devices and communicate the status back to the control unit. Two outputs are also available for controlling bells, lights, Led's, door locks, etc. These outputs are controlled from the control unit via the 2-wire cable.

The CS-212 is a 14,000 squaremill I^2L/Linear IC consisting of approximately 275 I^2L Gates, 100 BiPolar Transistors and 40 Resistors.



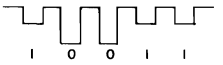
NOTES:
1. * indicates, IN 1 & loop IN 2, IN 3 cannot be used at the same time.
2. This diagram shown CS-212 circuit coded to #24.

2-WIRE TRANSMISSION CABLE (The Line)

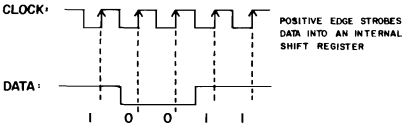
The 2-wire bidirectional transmission cable called "The Line" provides power and data to the CS-212 and also provides data back to the control circuit.

The line signal is rectified and filtered at each CS-212 and is used for the power supply to the chip. The CS-212 also decodes the line signal into clock and data signals used inside the IC.

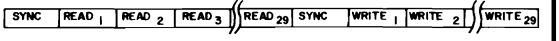
A typical line signal from the control unit would look like the following:



The CS-212 would decode this into clock and data.

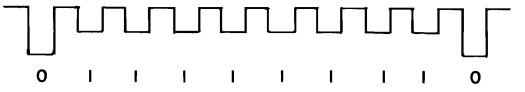


The CS-212 accepts addresses and commands in 10-bit word formats. Three types of words must be generated: Sync, Read and Write.



SYNC WORD

Synchronization is obtained by providing the CS-212 with 8 or more 1's followed by a "0" To prevent a false sync, it is best to send 0 before the 8 1's. This word insures all circuits on the same line see the commands at the proper time.

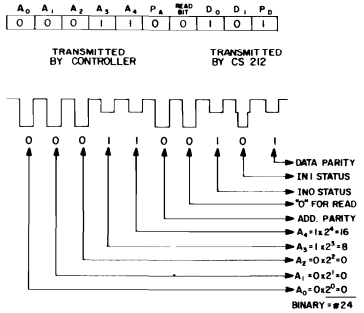


READ WORD

To check the status of a CS-212's inputs; i.e., IN0 and IN1 or IN2/IN3, a read word must be sent. The first 5 bits must correspond to the address of the CS-212 to be interrogated. Bit #6 is the address parity bit. It must insure that the first 6 bits are an even number of "1" 's. If the parity is even and the CS-212 to be interrogated has not previously received a parity error (odd parity), it will transmit its status, along with an internally generated parity bit. D_0 corresponds to IN_0, D1 corresponds to IN1 or IN2/IN3. After the address parity has been transmitted, the controller must allow the CS-212 to transmit. The controller must pull the line down to approximately 7.5V, then the CS-212 will transmit. If a "1" is to be transmitted, no change will occur on the line. If a "0" is to be transmitted, the CS-212 will then pull the line down. In either case, the controller must pull the line back up to 15V in order to continue. If the CS-212 has received a parity fault, it will transmit 3 one's (D0=D1=pD=1). This will allow the controller to detect a parity error. If a parity error is detected by the controller, the read word must be repeated.

TYPICAL READ WORD

Assume that Device #24 is to be interrogated and the status of IN0=1 and IN1=0.

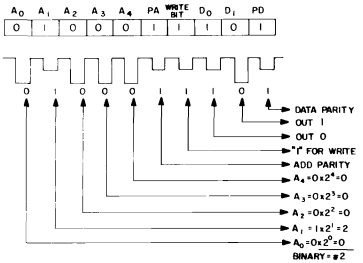


WRITE WORD

In order to update Out 0 and Out 1, a write word must be sent to the CS-212. The first 5 bits must correspond to the 212 you wish to update. Bit #6 is and address parity bit. It must insure even parity. D0 corresponds to Out 0 and D1 corresponds to Out 1. An even data parity bit must be received by the CS-212. If the address and data parity are even and the CS-212 has not previously received a parity error, it will update Out 0 and Out 1. If a parity error was received, the 212 will not be updated. In this case, a read word must be sent to clear the parity fault.

TYPICAL WRITE WORD

Assume CS-212 #2 is to be updated so that Out 0=1 and Out 1=0.

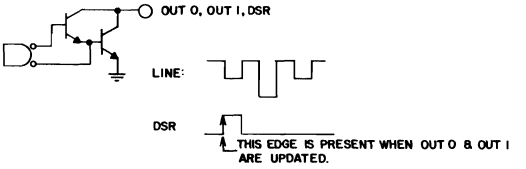


OUTPUTS

1 Out 0 and Out 1: Pin #'s 1, 16:
These outputs are updated according to the information present during the write word.

2. DSR: Pin #15:
The DSR pin is a monitor of the clock signal for the On Chip D type Flip Flops, corresponding to Out 0 and Out 1. It can be used to strobe data from Out 0 and Out 1 into external circuitry connected to the CS-212.

These three outputs can sink up to 1mA at 1.2V. They are Darlington type open collector outputs.



3. Data Out: Pin #11:
The Data Out is used to transmit the status of In 0 and In 1 to the line. For Data=1, the line driver is off. For Data=0, the line driver is turned on. This output is a saturated switch capable of sinking 10mA DC at .4V and 50mA at 1V on a transients basis. The 50mA is needed to discharge the line capacitance. A 150 Resistor from the line to Pin 11 limits the current into Pin 11 when the line driver is on.

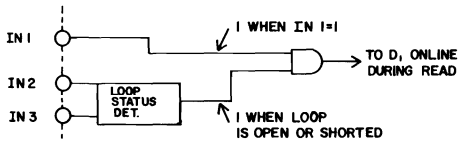
INPUTS

1. Address Inputs: Pin #'s 2, 3, 4, 5, 6.
The 212 has 5 address inputs which decide what address code it will respond to. Their thresholds are approximately 1/2 V_{DD} and draw less than 20uA. The inputs should be grounded for Logic 0 and tied to V_{DD} (Pin 12) through a 10K Resistor. The resistor is necessary for non-destruction of the IC with 28V applied to the line.

2. Data Inputs: Pin #'s 7, 8.
IN0 and IN1 (Pins 8 and 7) are digital inputs and are similar to the address inputs in that they have a threshold of approximately 1/2 V_{DD}. When the CS-212 is unaddressed, these inputs draw less than 20uA. When the circuit powers up, IN0 and IN1 source typically 400uA.

3. Detector Loop: Pin #'s 13, 14.
IN2 and IN3 can be used together to form a detector loop. When used, the outputs are connected together through a window foil and a diode. These inputs will generate a 1 at D1 on the line when the pins are shorted or opened.

When using IN2 and IN3, IN1 must be terminated to V_{DD} through the 10K Resistor used for the address inputs. When using IN1, IN2 and IN3 must be shorted or opened.



4. Line Input: Pin #9
The line input is internally connected to two comparators. These comparators separate the line signal into clock and data. The line input will draw less than 16uA of input current.

5. V_{DD}: Pin #12
The V_{DD} Pin provides power to the CS-212 circuitry. The line signal is externally rectified and filtered, then applied to V_{DD}. The V_{DD} pin draws varying amounts of current, depending upon the state of the 212. (See specification). The unaddressed current in less than .8mA.

The operating voltage range is 10V to 18V on Pin 12 of the IC. This wide range is necessary because of losses in the line and ripple on V_{DD}.

The circuit is designed to withstand 28V applied to the line. This is to prevent the destruction of the IC and its external components if the 2-wire cable is miswired.

7

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-212N	16 Lead PDIP

CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
(401) 885-3600 Telex WUI 6817157

Our Sales Representative in Your Area is:

CHERRY SEMICONDUCTOR

CS-235

SYSTEM PHOTOELECTRIC SMOKE DETECTOR

DESCRIPTION

The CS-235 System Smoke Detector is a photo electric type with a pulsed infrared LED as the light source and a silicon photodiode as the light detector. The CS-235 IC, along with passive external components, controls the system timing and signal processing.

Low average current is attained by pulsing the system once every 10 seconds for 20 milliseconds. Bias is applied to the signal processing circuitry for this time interval. During the second half of the pulse, the last 10 milliseconds, the IR LED is pulsed and the unit samples for an alarm level smoke condition. After the first alarm level signal the sample rate increases to a two second interval. After three consecutive alarm level samples the logic drives the output latch signalling the system panel.

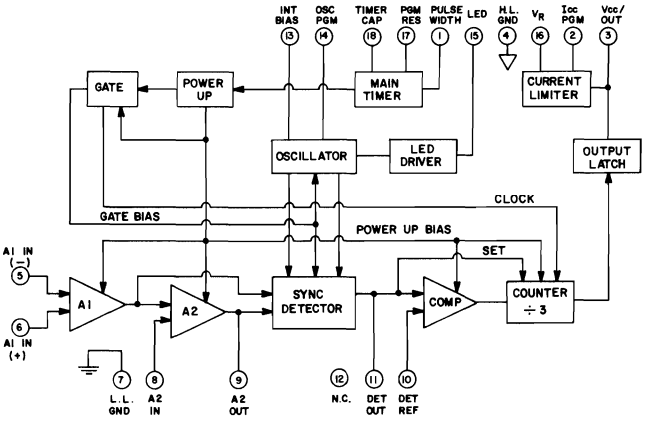
The signal processing circuit blocks are amplifiers A1 and A2, synchronous detector, voltage comparator and the decode counter. The voltage gain of A2 and the comparator reference voltage are set by external resistors.

Additional on-chip features include an I_{CC} current limiter The current limiter eliminates power-on false alarming.

The oscillator controls the IR LED excitation frequency and provides drive to the synchronous detector. The synchronous detection method has very high noise rejection performance.

The internal latch is capable of sinking 100 milliamps maximum and will clamp the V_{CC} pin to 5 volts when tripped. The latch current is determined by an external resistor typically located in the master panel and is reset by temporary removal of detector power.

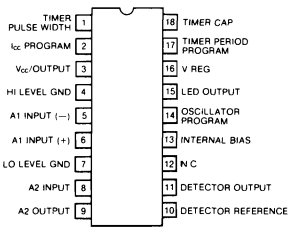
BLOCK DIAGRAM



FEATURES:

- Synchronous Detection for High Noise Immunity
- Pulsed Operation for Low Average Current Drain
- System Gain Externally Set
- System Sensitivity Externally Adjustable
- System Operation Monitored by means of External Red LED

PIN CONNECTIONS

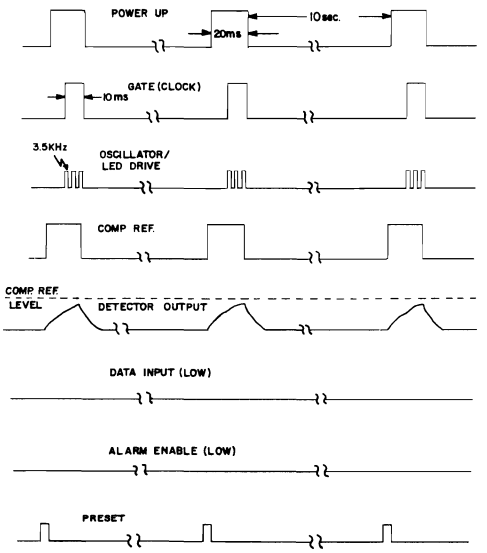


(TOP VIEW)

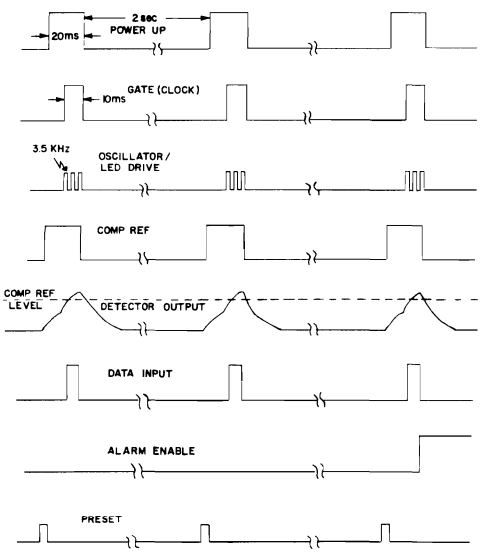
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating temperature range		-20		+70	°C
Absolute maximum voltage	(pin 3)			38	V
Output latch current				100	mA
24V System (C2 = 100 μF, R7 = 12 mΩ)					
Operating voltage	(pin 3)	13.8	22.5	35	V
Average supply current	V (pin 3) = 22.5V		35	60	μA
Peak supply current	V (pin 3) = 22.5V (non "speed up")			100	μA
Peak supply current	V (pin 16) = 12V ("speed up" mode)		150	350	μA
Regulator voltage	(pin 16)	12.8		15.7	V
12V System (C2 = 150 μF, R7 = 12 mΩ)					
Operating voltage	(pin 3)	8.7	12		V
Average supply current	V (pin 3) = 12V			60	μA
Peak supply current	V (pin 3) = 12V (non "speed up")			100	μA
Peak supply current	V (pin 16) = 8V ("speed up" mode)			350	μA
Regulator voltage	(pin 16) (V pin 3 = 12V)		11.85		V
Oscillator					
Output frequency	R6 = 18kΩ, C3 = .0068 μF	2.1	3.3	4.4	kHz
Sink current	(pin 14)	16	26	35	μA
Source current	(pin 14)	19	26	32	μA
High trip point voltage	(pin 14)	1.8	1.9	2.2	V
Low trip point voltage	(pin 14)	1.2	1.4	1.5	V
LED Drive (Detector LED and Status LED)					
Source current (pin 15)	R8 = 36 Ω				
Detector LED	V IR LED = 1.156V	20	30	40	mA
Status LED (alarm)	V status LED = 1.99V	10			mA
Regulator voltage (pin 15)	I_{SOURCE} = 30 mA	3.7	4.4	5.2	V
Amplifier A1					
Fixed gain			26		dB
Input current B1	(pin 5)		500	1000	nA
Input current B2	(pin 6)		500	1000	nA
Input current (B1-B2)				250	nA
Amplifier A2					
D.C. Output (pin 9)	R3 = 6 kΩ, R4 = 510 Ω, C5 = .47 μF		2.5		V
Input bias current (pin 8)	(Externally adjusted gain with R_3 and R_4. Unity D.C. gain)			250	nA
Voltage gain @ 3.5 kHz			21.6		dB
Detector and Reference Output (C4 = .47 μF)					
Reference resistance		13	19	25	kΩ
Reference voltage	(pin 10)	1.8	3.6	5.5	V
Detector output resistance		10	15	20	kΩ
Detector output voltage	(pin 11) (no signal, and at 2X time constant)	1.4	2.8	4.3	V
Main Timer (R1 = 20 mΩ, R2 = 75 kΩ, C1 = .47 μF)					
Power up pulse period	Standby mode (pin 1)	8	10	12	SEC
Power up pulse period	Speed up mode (pin 1)	1.5	2	2.5	SEC
Power up pulse width	(pin 1)		20		ms
Gate pulse width	Power up pulse width 12		10		ms
Sink current (pin 18)	V (pin 16) = 16V	415	460	505	nA
Source current (pin 18)		-220	-235	-250	μA
Output Circuit					
Output latch voltage	(pin 3) I_{SUPPLY} = 100 mA	4.4	5.2	6.1	V
Leakage current	V (pin 3) = 38V, V (pins 2, 16) = 0V		500		μA
Alarm					
Alarm reset	Supply interruption			5	SEC
Power up time				30	SEC
System will go into alarm upon detection and transfer of three consecutive alarm level signals into the counter.					

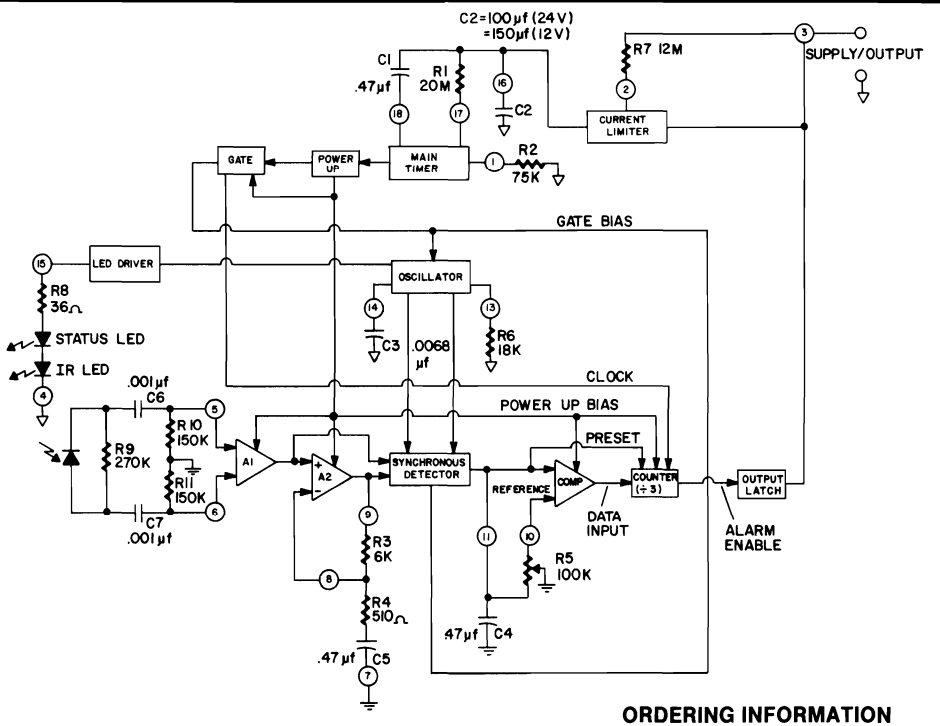
7



TIMING DIAGRAM
OUT OF ALARM



TIMING DIAGRAM
IN ALARM



SCHEMATIC DIAGRAM

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-235	18 Lead PDIP

CSC™ CHERRY SEMICONDUCTOR

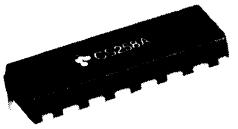
CS-258A

OPTICAL TRANSCEIVER

DESCRIPTION

The CS-258A is an LSI Integrated Circuit using Bipolar Linear/ Digital technology to combine power, low noise and logic functions. It is designed for use as an Intrusion Alarm, Proximity Detector or Small Particle Sensor in security, industrial or environmental applications.

With the addition of an IR LED, Photo Diode and several non-critical resistors and capacitors, the CS-258A becomes a complete optical transceiver system. It provides a 3-pole filtering network on the detector amplifier which reduces the response to 120Hz ambient light. This filtering, combined with gated detection of incoming pulses and multiple pulse integration requiring consecutive pulses for triggering, allows the designer to make his system relatively open to ambient conditions without false alerts.



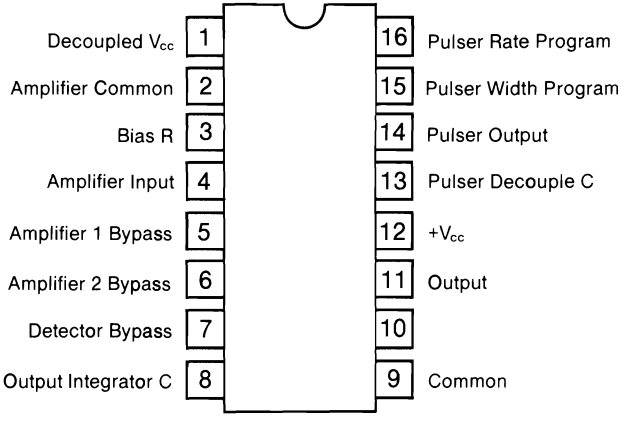
FEATURES:

- Gated Detector
- Combined Analog & Digital Noise Filter to eliminate false triggering
- On Chip 700mA Pulser
- On Chip 400μV Receiver
- On Chip Output Driver
- Ambient Light Operation
- Variable Frequency & Duty-Cycle Operation
- Reverse Polarity Protection

APPLICATIONS:

- Intrusion Alarm
- Particle & Dust Monitor
- Traffic Counter
- Inventory Control
- Production Counter

PIN CONNECTIONS



(TOP VIEW)

7

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL SPECIFICATIONS: Unless otherwise specified, V_{cc} = 6.0V, T_A = 25°C, and measurements are performed in the Applications Circuit of Fig. 2.

PARAMETER	MIN	TYP	MAX	UNITS
Operating Voltage	3.8	6.0	7.0	V
Supply Current (Less pulsed currents)	—	230	250	μA
Pulser on Time	18	20	22	μS
Pulser Rep. Rate	1.6	2.0	2.4	S
Pulser Output Current	500	675	1000	mA
Amplifier Trip Point	—	140	—	μV
Reverse Battery Current	2	75	120	mA
Load Drive (V_{OUT}=1.5V)	50	70	100	mA
Operating Temperature	-20	—	+55	°C

APPLICATIONS NOTES

Figures 1 & 2 show typical applications circuits with external component values.

TRANSMITTER:

The LED pulse period and width are established by an internal timer. Standby pulse period is a function of external components R2 and C1 according to the formula T=(0.7) (R2) (C1).

Pulse width is controlled by R_1 and C_1 and given by the formula T=(0.7) (R_1 + 60Ω) (C_1).

RECEIVER:

The receiver chain consists of two signal amplifiers, detector, receiver logic, integrator, comparator and output driver.

R3 provides bias current for the input amplifiers. The photodiode is loaded by R4, and the signal coupled to the amplifiers through C2. The amplifiers are AC coupled to provide rejection of background DC and low frequency light. C3 and C4 bypass the amplifier bias networks. R5 establishes the gain of the first amplifier. C5 bypasses the detector reference.

The detector output is processed through a logic network that enhances noise immunity and assures the recognition of only data that is in synchronism with the transmitted pulse. Valid detector output information is then integrated to provide further noise immunity and control the system response time characteristics. C8 is the integrator capacitor.

R6 programs internal current sources that determine the standby operating currents.

ORDERING INFORMATION

Part Number	Description
CS-258A	16 lead PDIP

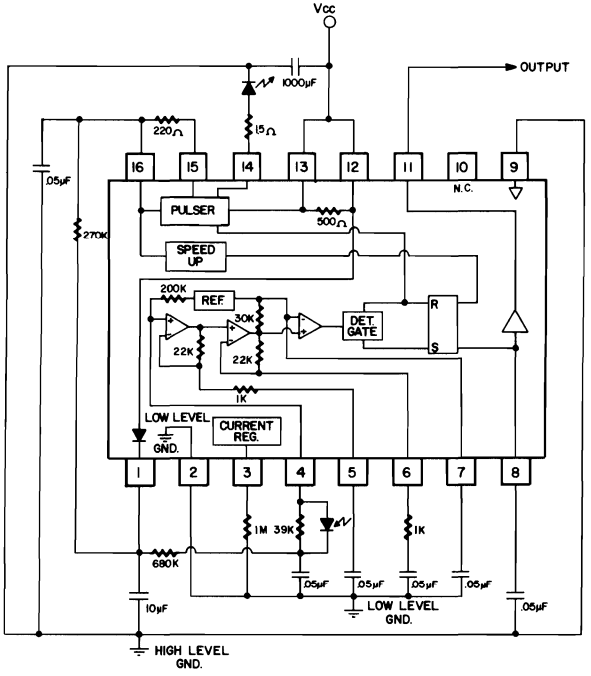


Figure 1. TYPICAL APPLICATION WITH ON CHIP LED DRIVE

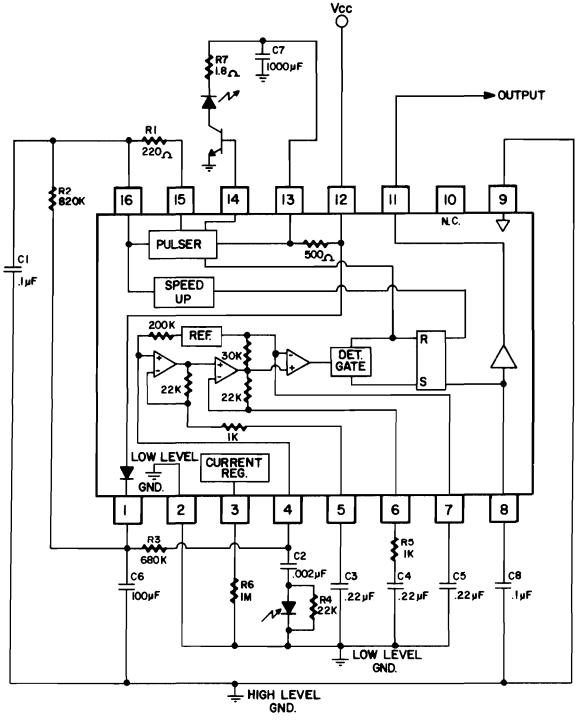


Figure 2. TYPICAL APPLICATION WITH EXTERNAL LED DRIVE

7

CSC™ CHERRY SEMICONDUCTOR

CS-2516

PULSE-LOAD BATTERY MONITOR

DESCRIPTION

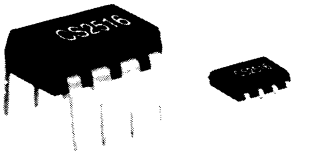
The CS-2516 is designed for use in battery powered medical, security, or environmental systems where prior notification of impending power source failure is a requirement. The IC effectively provides continuous monitoring of battery condition by pulse-sampling the system voltage at predetermined intervals. Low standby current permits unswitched connection to the battery with minimal impact on operating life. The ability to load the battery during the test pulse provides assurance that sufficient reserve capacity exists to operate critical system components.

The CS-2516 contains an internal timer that generates a 1.5 millisecond test pulse once each 45 seconds (both times are typical). The load switch transistor conducts only during the test pulse, and can sink up to 50 mA directly. An external transistor can be added to increase the load current capability.

Should, during the test pulse, the sense terminal voltage fall below the threshold level determined by the internal (synthesized) temperature compensated zener diode, the comparator will permit a charging current to flow out of pin 7. This pin is also the input of a Schmitt trigger that in turn drives the output transistor. Collectively, the charge current and trigger, in conjunction with an external RC network, operate as a "pulse-stretcher" to provide output "on" times that are a multiple of the sampling time. This feature permits low battery alarm devices or visible annunciators to be driven directly by the IC. The maximum permissible output current is 30 mA.

ABSOLUTE MAXIMUM RATINGS

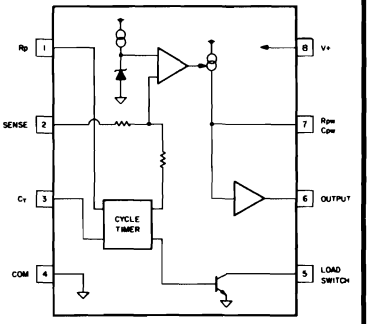
	MIN	MAX	UNITS
Supply voltage (Vcc, V8)	0	14	V
Cp pin voltage (V7)	-0.5	2.6	V
Terminal voltage (V1, V2, V3, V5, V6)	-0.5	V8	V
Load current (I5)		50	mA
Output current (I6)		30	mA
Operating temperature	0	+85	C
Storage temperature	-40	150	C
Soldering temperature (10 seconds max)		300	C



FEATURES:

- Adjustable battery sense from 7 to 12 volts
- Pulse-loads battery at up to 50mA
- Standby current under 10μA
- Test period, rate and load adjustable
- On chip 30mA output driver
- 8 lead plastic DIP
- SO-8 miniature plastic

PIN CONNECTIONS



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

ELECTRICAL CHARACTERISTICS Unless otherwise noted, V8=9V, Rp=9. 1 Mohm, CT=4.7uF, Cpw=0.1uF, Rpw=10Mohm

PARAMETER	PIN	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	(Is)	V8=12V, Is=(I2+I5+I6+I8)		5	10	uA
LOAD CYCLE TIMER						
Charge Current	3 3	V3=0V V3=7.5V	0.64		1.03	uA uA
Discharge Current	3 3	V3=8.8V V3=2V	8 1.1	3.6	25 mA	mA
LOAD SWITCH						
"ON" Voltage	5	V3=9V 15=50mA		0.5	0.7	V
"OFF" Current	5	V3=1.5V V5=12V			2	uA
SENSE INPUT						
Threshold Voltage	2	V3=4.5V	6.3	6.7	7.1	V
Threshold Tempco	2	T=OC to +85C		150		PPM/C
Input Current	2	standby, Vw=0 to V8			1	uA
Input Resistance	2	active	5	8.5	12	Kohms
PULSE STRETCHER						
Source Current	7	V2=6V V7=0V	400	500		uA
Input Bias Current	7	V2=V8 V7=3V			1	uA
OUTPUT SWITCH						
"ON" Voltage	6	V2=V8=6V V3=4V I6=15mA V7=3V		0.25	0.5	V
"OFF" Current	6	V2=V8=6V V3=4V V6=12V V7=1V			1	uA

APPLICATIONS INFORMATION

Refer to typical applications circuit (all values are approximate):

Test cycle period (seconds) = Ct (farads) / Rp (ohms)
Test pulse width (milliseconds) = 0.3 x Ct (uF)
Output pulse width (seconds) = 0.25 x Rpw x Cpw (megohms, uF)
Typical standby current (microamps) = (3.5 x (V8 / Rp)) + 1 where Rp is expressed in megohms.

Component selection notes:

(Rp) The value of Rp affects standby current, operating current, and the test cycle period. The recommended value is (V+/1uA), where (V+) is the fresh battery voltage. Higher values are not recommended; minimum recommended value is (V+/10uA), which will both increase standby current and reduce test period by 10X.

(Ct) The value of Ct affects both the test period and test pulse width. Of critical importance is the selection of a low leakage current capacitor. With Rp dimensioned according to the formula (V+/1uA), the capacitor charging current is approximately 1uA. If the leakage current exceeds the charge current, the cycle timer will not operate. The range of practical values is 4.7uF minimum, 22uF maximum.

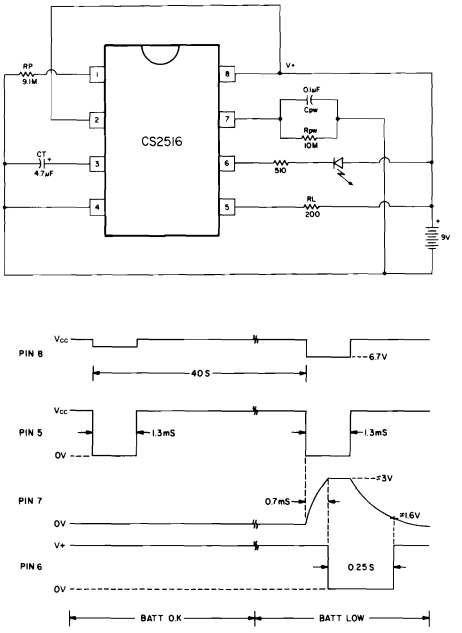
(Rpw & Cpw) The recommended range of values is 1 to 10 megohms and 0.01 to 0.1 uF.

Threshold voltage modification:

The effective low battery threshold voltage can be modified (increased only) by means of a voltage divider placed across the load resistor. This technique can also be used to effectively reduce the threshold tolerance band.

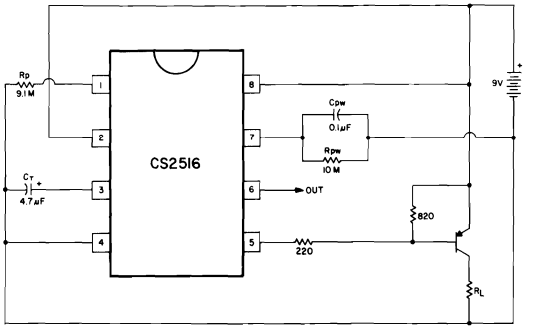
APPLICATIONS

FIGURE 1



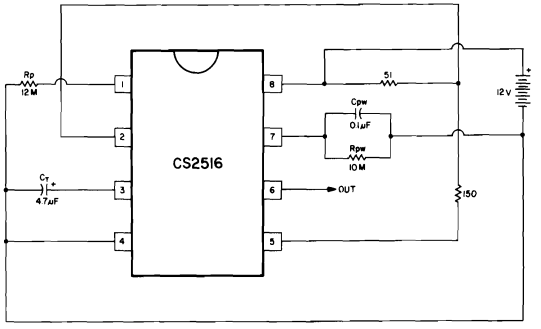
TYPICAL APPLICATION CIRCUIT AND WAVEFORMS

FIGURE 2



INCREASED PULSE-LOAD CURRENT CAPABILITY

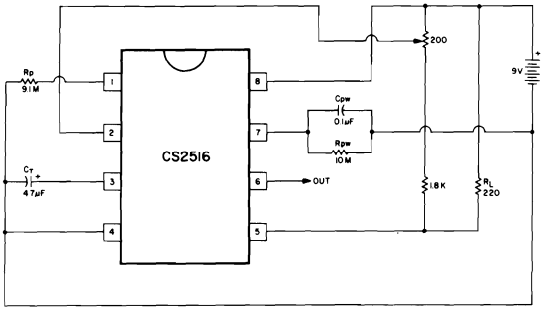
FIGURE 3



12 VOLT BATTERY APPLICATION WITH 9V THRESHOLD

APPLICATIONS cont.

Figure 4



ADJUSTABLE SENSE THRESHOLD

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-2516N	8 Lead PDIP
CS-2516D	8 Lead SO

7

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

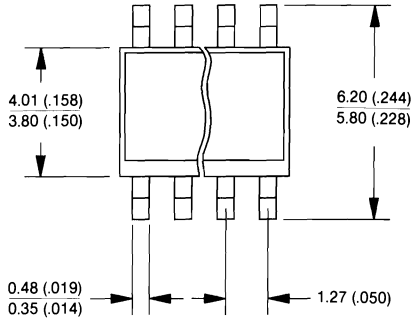
Our Sales Representative in Your Area is:

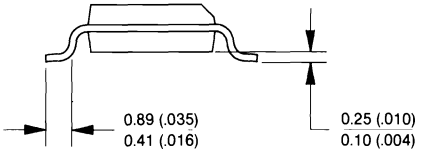
PACKAGE SUFFIXES

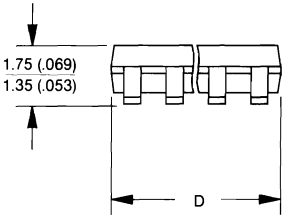
Letter Designator	Package Type
N	Plastic DIP
J	Ceramic DIP
V	Multiwatt Vertical
VH	Multiwatt Horizontal
FN	PLCC
D	SO Surface Mount Narrow
DW	SO Surface Mount Wide
T	TO 220
Z	TO 92

SO - Narrow
DIMENSIONS IN MM (INCHES)
Package Suffix-D

LEAD COUNT	D			
	METRIC		ENGLISH	
	MAX.	MIN.	MAX.	MIN.
8	5.00	4.80	.197	.188
14	8.74	8.53	.344	.336
16	10.00	9.80	.394	.385

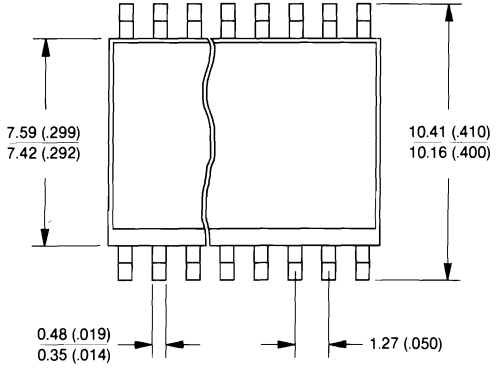


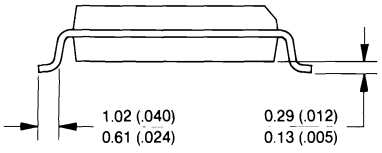


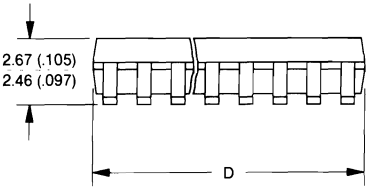


SO Wide
DIMENSIONS IN MM (INCHES)
Package Suffix-DW

LEAD COUNT	D			
	METRIC		ENGLISH	
	MAX.	MIN.	MAX.	MIN.
16	10.46	10.21	.412	.402
18	11.71	11.46	.461	.451
20	12.95	12.70	.510	.500
24	15.54	15.29	.612	.602
28	18.06	17.81	.711	.701

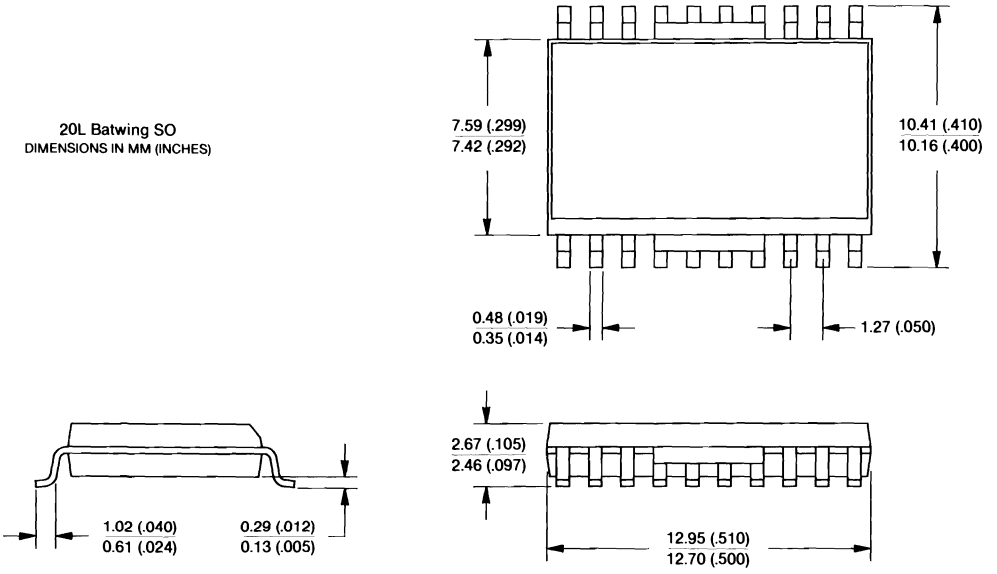




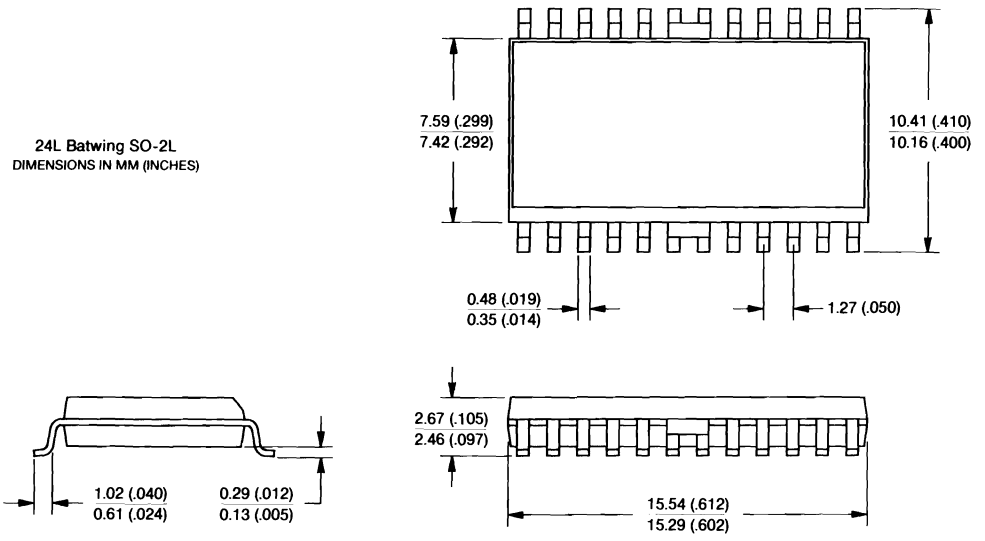


8

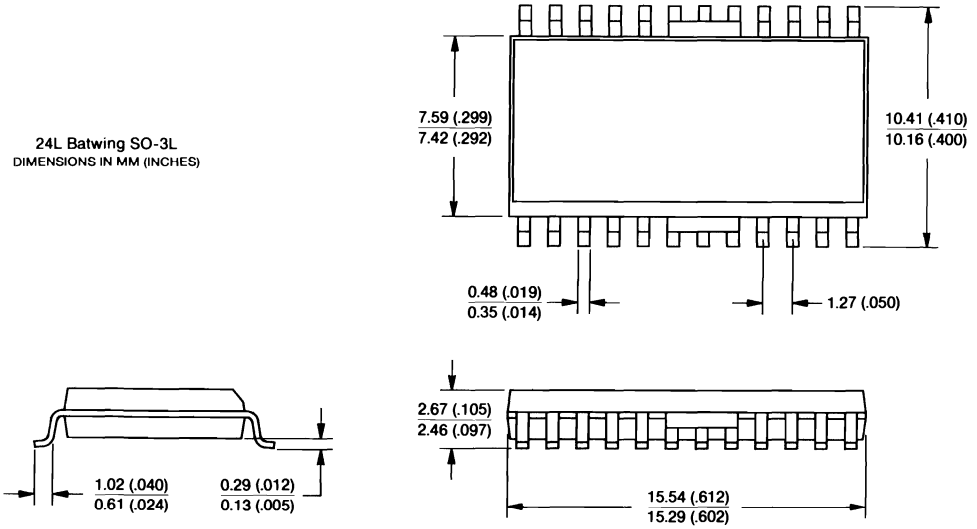
20L Batwing SO
DIMENSIONS IN MM (INCHES)



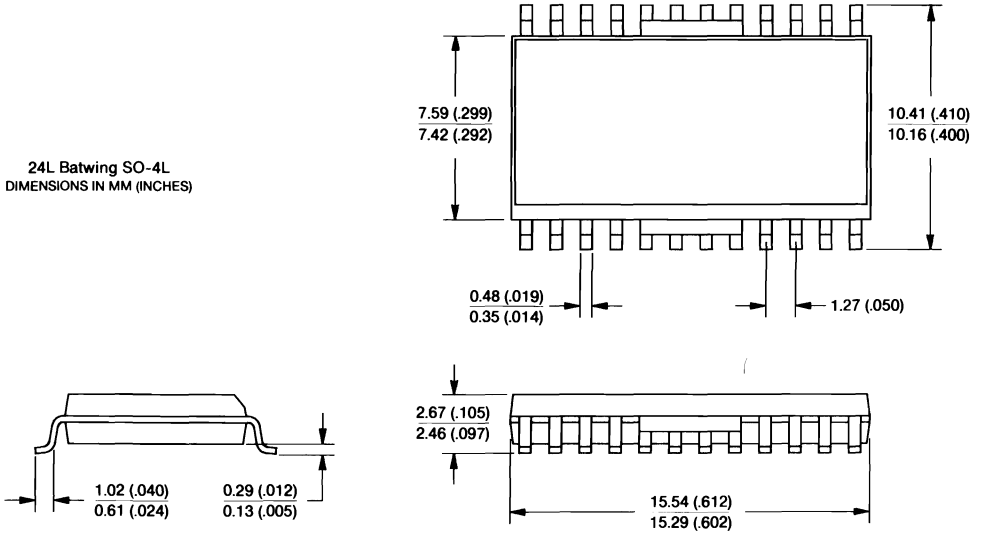
24L Batwing SO-2L
DIMENSIONS IN MM (INCHES)



24L Batwing SO-3L
DIMENSIONS IN MM (INCHES)

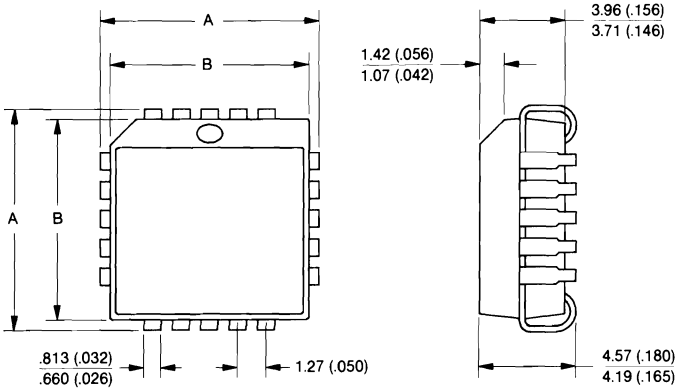


24L Batwing SO-4L
DIMENSIONS IN MM (INCHES)



8

PLCC
DIMENSIONS IN MM (INCHES)
Package Suffix-FN

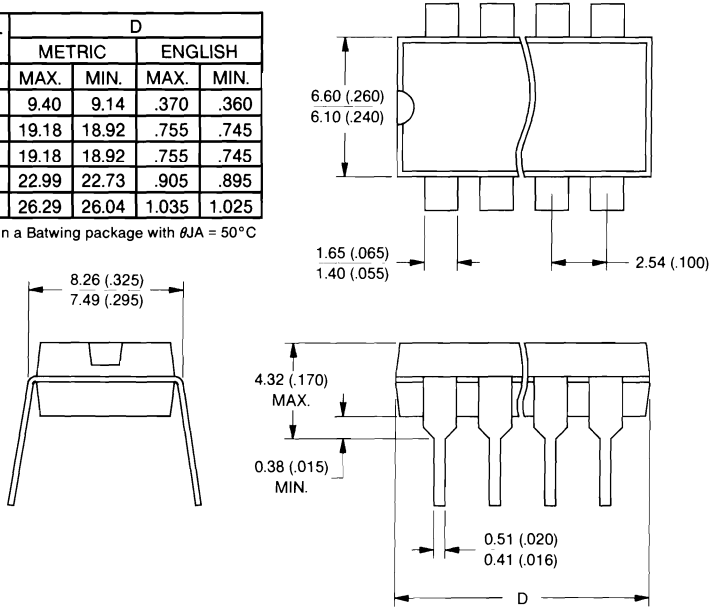


LEAD COUNT	ENGLISH				METRIC			
	A		B		A		B	
	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.
20	.395	.385	.354	.350	10.03	9.78	8.99	8.89
28	.495	.485	.454	.450	12.57	12.32	11.53	11.43
44	.695	.685	.654	.650	17.65	17.40	16.61	16.51
68	.995	.985	.954	.950	25.27	25.02	24.23	24.13

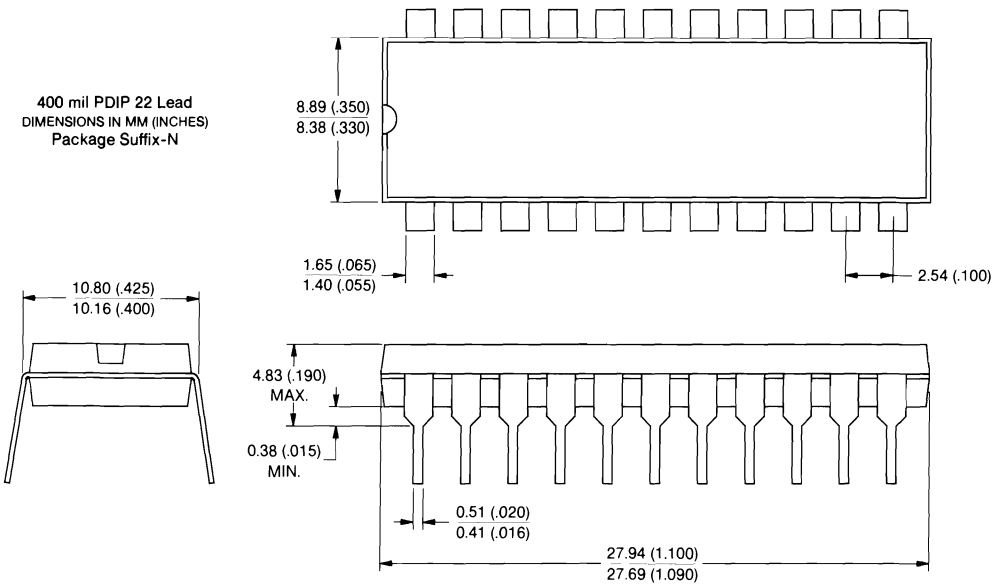
300 mil PDIP
DIMENSIONS IN MM (INCHES)
Package Suffix-N

LEAD COUNT	D			
	METRIC		ENGLISH	
	MAX.	MIN.	MAX.	MIN.
8	9.40	9.14	.370	.360
14	19.18	18.92	.755	.745
16*	19.18	18.92	.755	.745
18	22.99	22.73	.905	.895
20	26.29	26.04	1.035	1.025

* Also available in a Batwing package with θJA = 50°C Watt



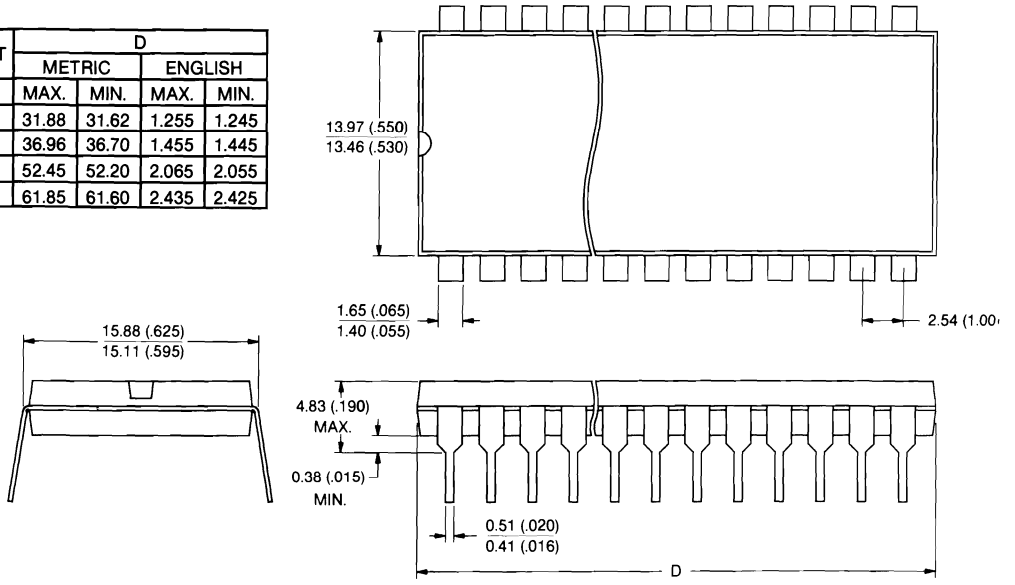
400 mil PDIP 22 Lead
DIMENSIONS IN MM (INCHES)
Package Suffix-N



8

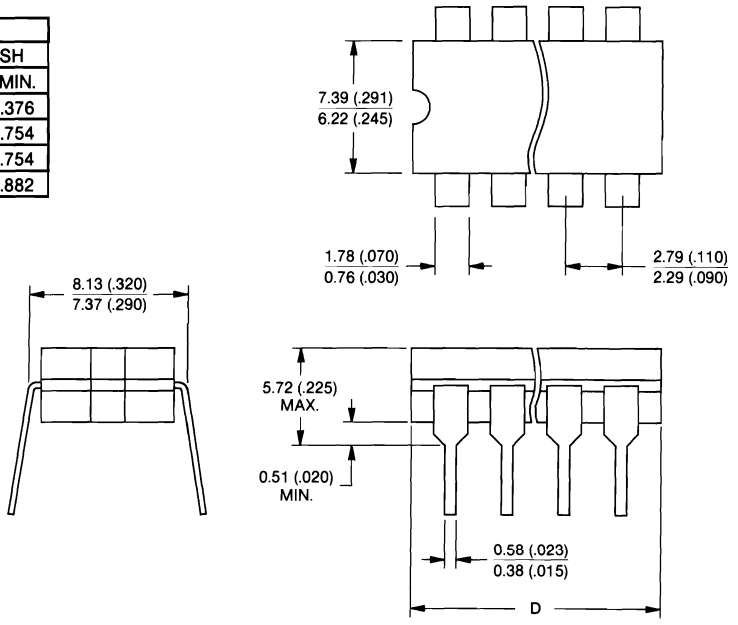
600 mil PDIP
DIMENSIONS IN MM (INCHES)
Package Suffix-N

LEAD COUNT	D			
	METRIC		ENGLISH	
	MAX.	MIN.	MAX.	MIN.
24	31.88	31.62	1.255	1.245
28	36.96	36.70	1.455	1.445
40	52.45	52.20	2.065	2.055
48	61.85	61.60	2.435	2.425



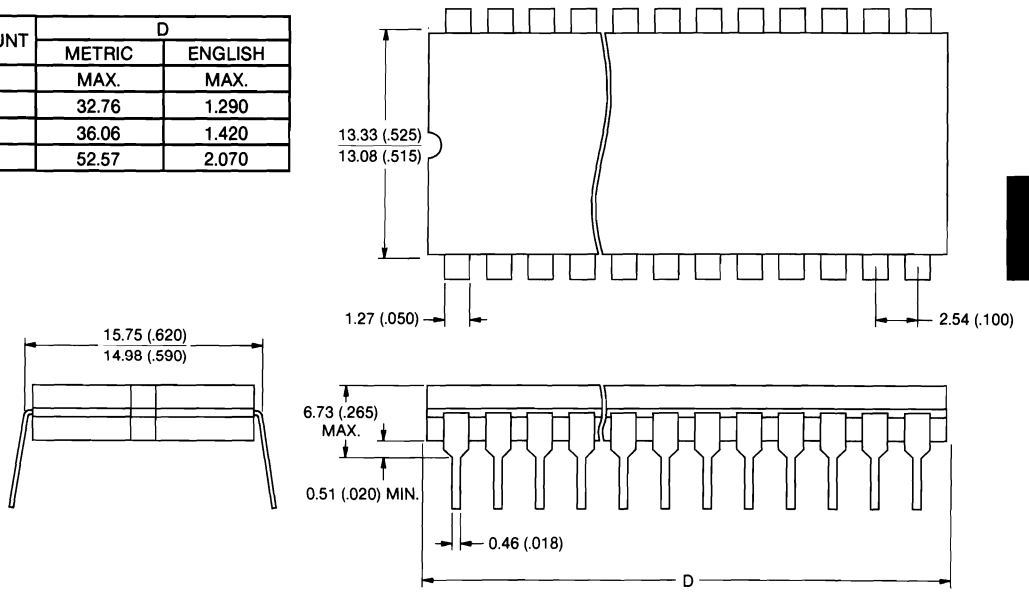
CERDIP 300 mil
DIMENSIONS IN MM (INCHES)
Package Suffix-J

LEAD COUNT	D			
	METRIC		ENGLISH	
	MAX.	MIN.	MAX.	MIN.
8	10.29	9.55	.405	.376
14	19.94	19.15	.785	.754
16	19.94	19.15	.785	.754
18	23.50	22.40	.925	.882



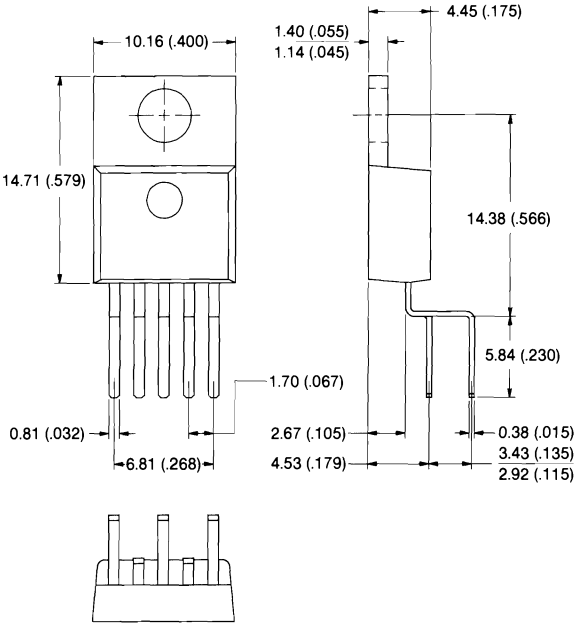
CERDIP 600 mil
DIMENSIONS IN MM (INCHES)
Package Suffix-J

LEAD COUNT	D	
	METRIC	ENGLISH
	MAX.	MAX.
24	32.76	1.290
28	36.06	1.420
40	52.57	2.070

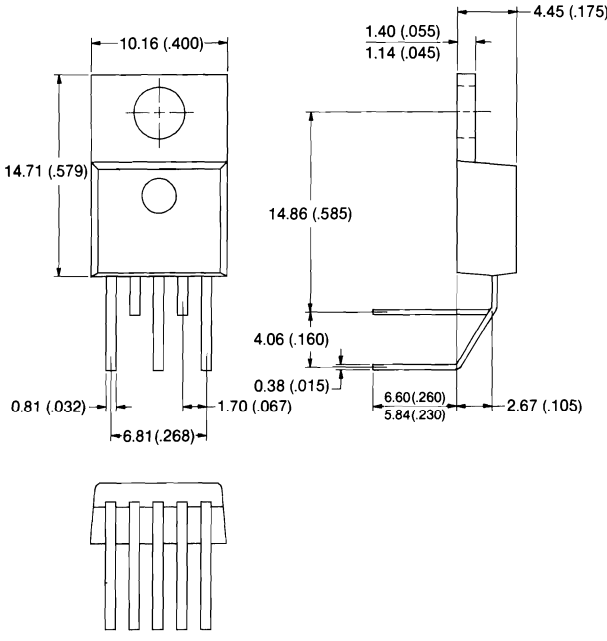


8

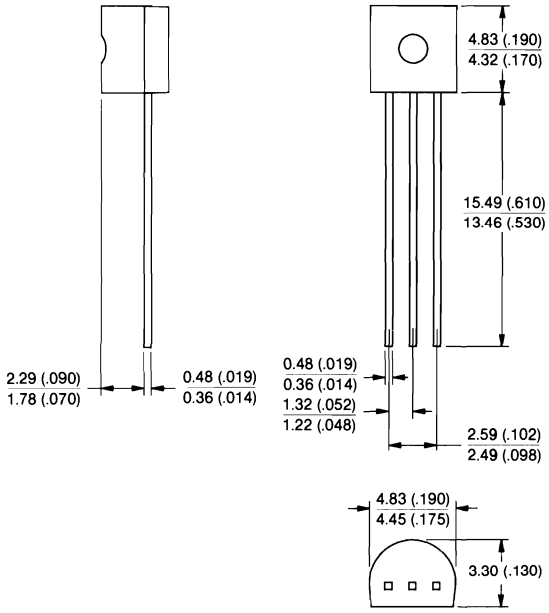
TO-220 (Vertical)
DIMENSIONS IN MM (INCHES)



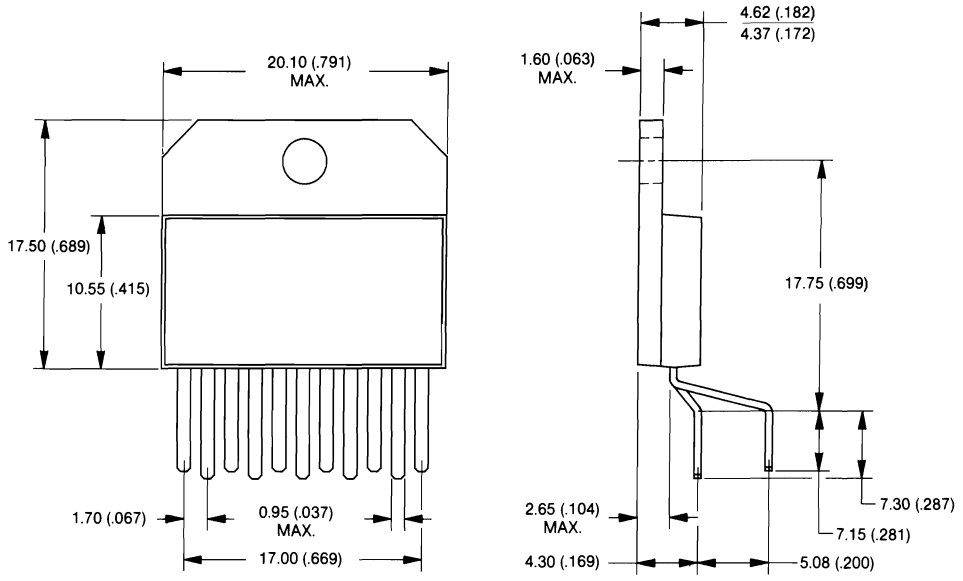
TO-220 (Horizontal)
DIMENSIONS IN MM (INCHES)



TO-92
DIMENSIONS IN MM (INCHES)
Package Suffix-Z

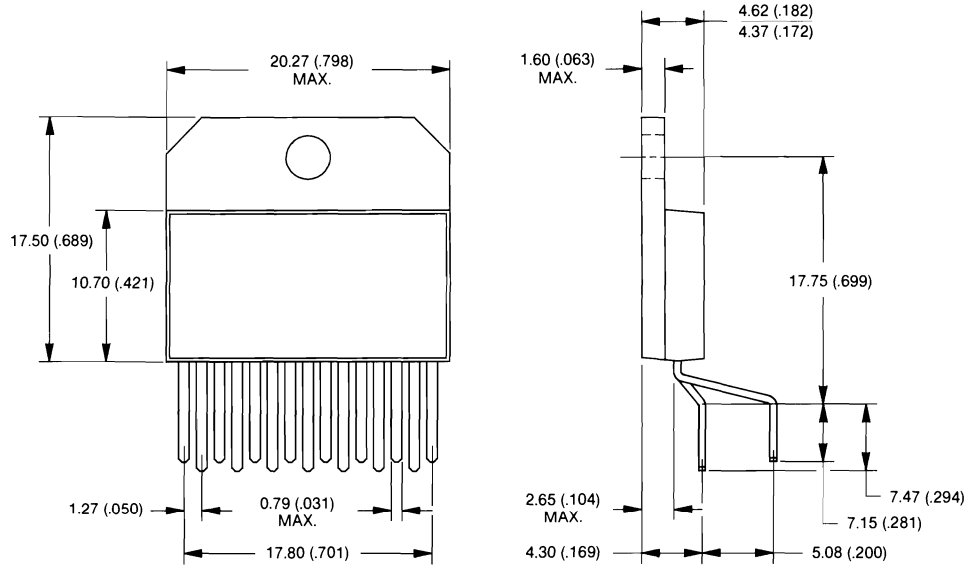


11 Lead SIP (Vertical)
DIMENSIONS IN MM (INCHES)
Package Suffix-V

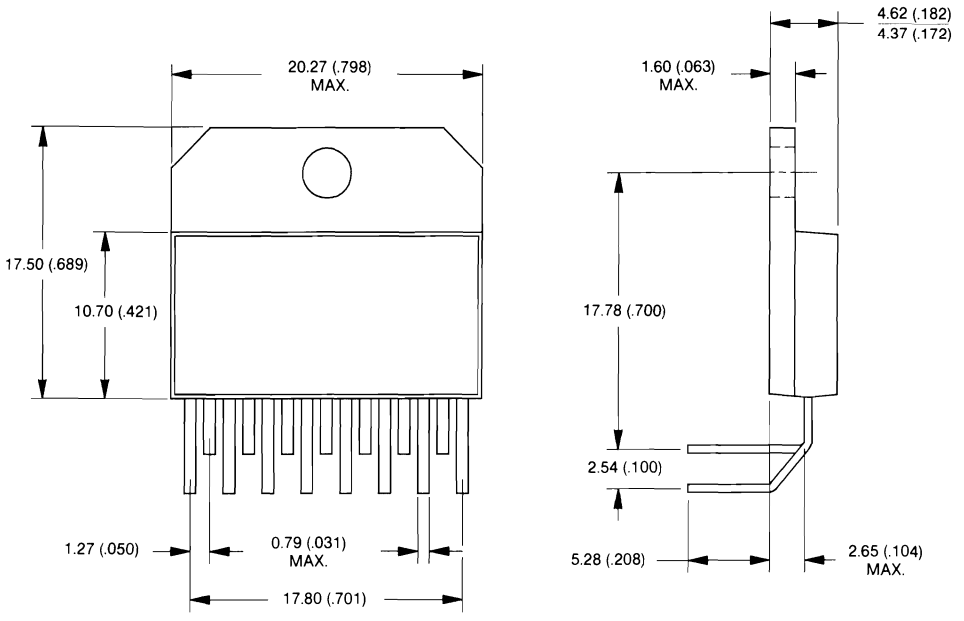


8

15 Lead SIP (Vertical)
DIMENSIONS IN MM (INCHES)
Package Suffix-V



15 Lead SIP (Horizontal)
DIMENSIONS IN MM (INCHES)
Package Suffix-VH



SEMICUSTOM BIPOLAR ARRAYS

INTRODUCTION

'REFACE

The almost incredible growth of electronics technology ınd applications over the past twenty years is directly elated to the developments that have taken place in the emiconductor industry. Indeed, none of the electronic ronders we now take for granted would have been ossible without the transistor, and in particular, the ıtegrated circuit.

With the ever increasing variety of circuit applications, ountless numbers of standard devices have been intro- luced in an attempt to satisfy the multitude of design roblems. While practically all circuit applications can be atisfied with standard integrated circuits and/or discrete evices, in many situations they are a compromise that ıay prove unacceptable in terms of functional perfor- ıance, cost, or required board space.

:USTOM CIRCUITS

Custom integrated circuits can offer significant advan- ıges to the circuit designer. A full custom circuit is chosen or specific reasons, and usually when substantial roduction runs are expected. While engineering and ooling charges are a one-time cost, they can be ubstantial. It is to the users benefit that these costs be mortized over a large piece-part base. Where large uantity requirements exist, engineering charges become elatively insignificant, and low unit prices are realized. ;ustom circuits can be very cost-effective in combining iverse circuit functions, or in the replacement of several iscrete packaged functions with a single circuit, pecifically tailored to the customer's requirements. Some f the more important considerations in choosing a ustom circuit are itemized in the following list:

ıdvantages

. PROPRIETARY DESIGN: Unique circuit functions and combinations can be incorporated in a single chip.
. LOWER COSTS: By combining many functions on a single chip, assembly, test, handling, and inventory costs are all reduced, compared to separate discrete components.
. SPACE SAVINGS: Significant reductions in printed circuit area are usually obtained. In many applications this can be of singular importance.
4. HIGHER RELIABILITY: By reducing the number of individual circuits and connections there is a demonstrable improvement in overall system reliability.

Other considerations:

1. LEAD TIME: 40 to 50 weeks is typical, actual lead time depends on several factors such as circuit complexity.
2. ENGINEERING AND TOOLING COSTS: One time charge for design, layout, test programs and initial samples. Costs vary, but normally are justified only by large volume requirements.
3. MODIFICATIONS: Possible need to modify if first samples do not perform to exact specifications, resulting in extension of lead time.

For applications where only moderate production runs are anticipated, a custom circuit can sometimes be justified by the reduction in board space, handling, and inventory costs. In most cases, however, CSC would probably recommend that a semicustom alternative be considered.

SEMICUSTOM CIRCUITS

Semicustom ICs offer the advantages of a proprietary design at a fraction of the development time and tooling cost of a "full custom" circuit. Semicustom programs are better suited to those applications where moderate production volumes are required, and where short prototype lead time is important. Should future production levels increase, GENESIS™ ICs can be converted to full custom versions to achieve the lowest possible unit cost. Since the design is already proven, the conversion is essentially risk free.

CSC's semicustom design programs include conventional linear bipolar, integrated injection logic (I^2L) and specialized technologies such as Flip-Chip metallurgy, extended performance, optoelectronic sensors, ion implanted resistors, and linear/low power Schottky. Full details for all of the GENESIS semicustom circuits are provided in the selection guides, data sheets, and in the special sections on Digital and Linear applications.

NOTE: Available from CSC is a complete Semicustom Circuit Design book as well as a GENESIS™ onLine™ User's Manual. Contact local sales representative for information.

9

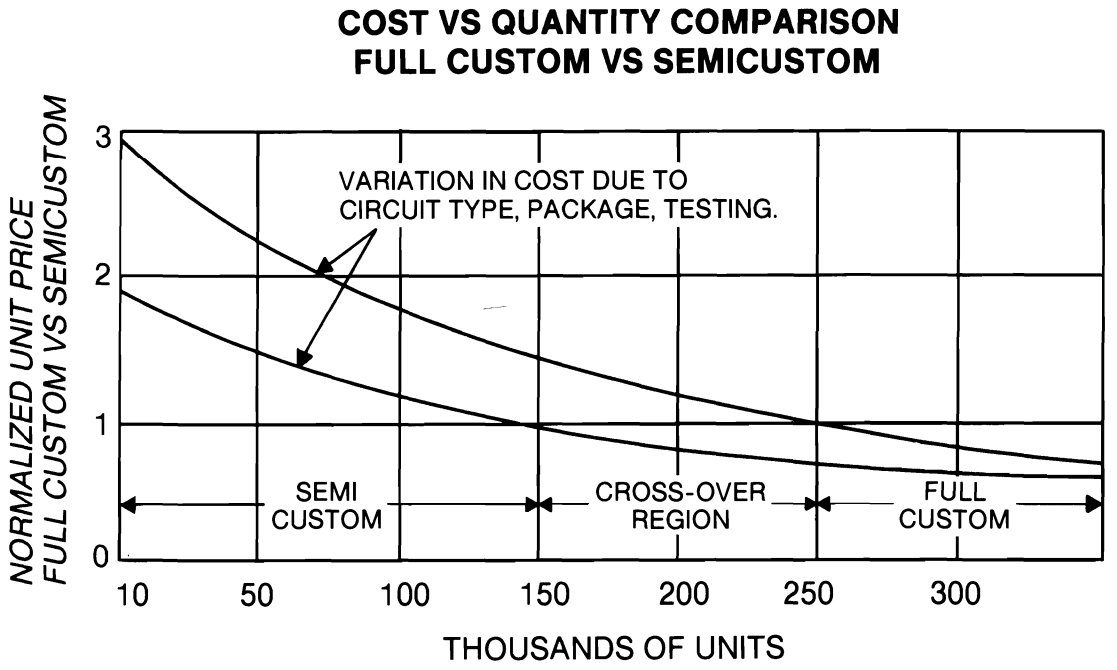
ECONOMICS OF SEMICUSTOM CIRCUITS

In general, a semicustom IC starts to become cost-effective when annual production quantities exceed 5000 units. While engineering and tooling charges are low compared with full custom circuits, the amortization of these charges is difficult to justify where only a few hundred circuits are required. The many advantages of semicustom ICs are normally best utilized in the range of 10,000 to 150,000 units.

Where production requirements are expected to be in the area of 250,000 units or more, it is nearly always more economical to design a full custom circuit. Full custom ICs will always be smaller than semicustom versions because of the higher density of integration attainable, and smaller chips mean lower unit prices. The amortization of engineering charges is also much easier to justify when spread over a large production base.

A "cross-over" region exists where expected production volume is in the range of 150,000 to 250,000 units. In this range, a number of factors can affect the decision as to whether a semicustom, or full custom circuit is the better choice. Among these are circuit complexity, expected yield, packaging requirements, and test specifications.

These relationships are illustrated in the following graph which projects the amortized unit cost ratio vs. the quantity of ICs produced.



For purposes of comparison the normalized unit price ratio is plotted against the quantity of ICs purchased. Where this ratio is greater than 1.0 the semicustom approach is more cost-effective.

1. Semicustom is more cost-effective for production quantities of 150,000 units, or less.
2. Full custom is more cost-effective for production quantities of 250,000 units, or more.
3. For quantities in the range of 150,000 to 250,000 units, the most cost-effective approach is dependent on circuit complexity, size of the chip, packaging requirements, test specifications, and expected yields.

LECTING A CHIP

emicustom chips vary in size, voltage ratings, number onding pads, and in the type and quantities of active d passive components. In general, the chip selected d be the smallest in die area that contains the mponents required for the intended application. The aller the die, the more die per wafer, and the lower cost. While it is not possible to utilize all components a chip, every effort is made to provide the optimum tch between the chip selected and the components ured by the customer's application. In most cases 65- % of the total chip area can be utilized, and occasionally re. This "underutilization" of chip area is one of the tors that makes the costs of semicustom circuits higher t full custom. The advantages of the semicustom ution are in the shorter lead time, and significantly lower gineering and tooling costs. The advantages of a prietary design, space savings, and higher reliability also retained.

For applications where both digital and analog functns are needed, the 1100, 1400 and 1500 offer a range potential functions. The 1100 is particularly useful, being marily a linear array to which has been added a cluster 64 I^2L gates. The gates are speed/power programmable m 100 to 2000 nA/gate with corresponding propogation lays from 7 to 0.05 usec. The linear components include 2 NPN transistors, 41 PNP transistors, and 347 resistors. ong the NPN transistors, 41 PNP transistors, and 347 sistors. Among the NPN transistors are Schottky-mped types for high-speed logic interfaces and "power nsistors with 400 mA capability. The 1400 contains 256 . gates, and a selectable mix of up to 69 transistors, d 200 resistors.

A wide selection of linear arrays are presently available, luding several that are unique to CSC.

The 2800 is available as an unpackaged Flip-Chip with tin/lead "solder bumps" for direct reflow-solder nding to hybrid substrates. Since wire bonds are minated, the 2800 offers enhanced reliability for critical plications such as underhood automotive electronics. e 2800 has a total of 333 components, including 85 nsistors and 248 resistors.

The 3100 uses a combination of diffused and ion implant sistors to open a new spectrum of applications for linear micustom ICs. With over 5 Megohms of resistance ailable from 355 total resistors, micropower functions e easily integrated. Active components include 88 NPN, d 36 PNP transistors.

The 3500 is a specialized chip designed for optoctronics applications. If features an integrated on-chip otodetector that can be connected as either a photode or phototransistor. In addition to the detector, which cupies approximately 11.5% of the total chip area, the 00 contains 299 components, including 85 transistors d 214 resistors. Applications of the 3500 encompass th linear systems and pulsed light-to-signal converters pable of operating at frequencies up to 100 KHz.

The 7600 L/LS circuit combines a high frequency linear cess with LSTTL gate equivalent capabilities. Active mponents include 138 small NPN transistors, 4 large NPN transistors, 26 PNP transistors, and 10 dual diodes. All NPN transistors can be selectively Schottky clamped to enhance switching speed. The gain-bandwidth product of the small NPN transistors is typically 800 MHz. The resistor complement includes 384 diffused resistors with a combined value of 525K, and 139 ion-implant resistors with a combined value of over 2 Megohms.The variety and characteristics of the 701 total components make the 7600 an especially versatile, and high performance chip for a wide range of linear applications.

The 2200E, 2500G, 3000F, 3200L, 3600, and 4000M are general purpose types, suitable for many diverse applications. Selection of a particular chip would be based primarily on the number and types of components needed for integration of the original circuit.

The 5000 features 8 power transistors that can be paralleled for up to 2 Amps of output current. Components are arranged in a array of 'macrocells' for ease in replicating functional circuit blocks.

EXTENDED PERFORMANCE OPTION

GENESIS linear ICs are available in a choice of two different wafer fabrication processes. The STANDARD option is the industry-standard seven mask epitaxial collector bipolar process utilized by the majority of linear semicustom manufacturers. This approach uses shallow emitter diffused underpasses in each transistor cell to provide the necessary conductor routing flexibility. Since the insulating oxide over the emitter diffusion is relatively thin, there exists a danger of electostatic discharge damage to the IC if a conductor to an input/output pin is allowed to pass over an emitter diffused underpass.

Available without extra cost on all GENESIS linear and linear/digital chips, the EXTENDED PERFORMANCE option adds an additional N+ collector wall diffusion to reduce the saturation resistance and extend the useful operating current range of NPN transistors. The shallow emitter diffused underpass regions of the standard process are eliminated and replaced with deep collector diffusions that provide a much thicker insulating oxide. Additional benefits of this option include lower underpass resistance and elimination of all layout restrictions regarding the routing of input/output conductors over emitter oxide.

BREADBOARD COMPONENTS

Designs are usually developed with either discrete components or transistor arrays. For those customers doing their own design, we recommend standard carbon film resistors and GENESIS monolithic breadboard components. These arrays are made directly from the appropriate GENESIS wafer and will assure the most accurate simulation of the completed semicustom IC. Breadboard components include both linear and digital types.

The linear transistor arrays contain 4 to 5 NPN or PNP transistors, with specific arrays having compatibility with specific semicustom circuits. A number of Design Kits are available that contain various quantities of the individual arrays for ease in breadboarding circuit functions to be incorporated in the selected semicustom chip. Complete details on the individual arrays, and the Design Kits are provided in the Selection Guides, and the section on Linear Programs.

GENESIS™ SEMICUSTOM BIPOLAR ARRAYS

TYPE NUMBER	ARRAY TYPE	DIE SIZE (Mils)	Vcc RANGE (V)	BOND PADS	I^2L GATES	DIODES	TRANSISTORS			RESISTORS		
							NPN	PNP	PWR NPN	DIFFUSED	ION IMPLANT	PINCH
1100	DIGITAL & LINEAR	102 x 127	1-12	26	64	—	98	41	4	339	—	8
1400	DIGITAL & LINEAR	120 x 150	1-12	40	256	—	UP TO 103 (ANY MIX)		—	UP TO 250		—
1500	DIGITAL & LINEAR	123 x 140	1-12	30	98	—	122	72	4	462	—	2
2200E	LINEAR	70 x 74	1-20	18	—	—	40	31	2	155	—	4
2500G	LINEAR	83 x 78	1-20	18	—	—	58	18	2	239	—	8
2800	LINEAR	80 x 85	1-20	16	—	—	58	25	2	240	—	8
3000F	LINEAR	91 x 113	1-20	24	—	—	97	39	4	416	—	10
3100	(MICROPOWER) LINEAR	83 x 111	1-20	22	—	—	85	36	3	86	261	8
3200L	LINEAR	83 x 111	1-20	22	—	—	85	36	3	347	—	8
3500	(OPTO) LINEAR ARRAY	75 x 97	1-20	22	—	—	59	24	2	206	—	8
3600	LINEAR	102 x 119	1-20	25	—	—	117	52	6	482	—	12
4000M	LINEAR	98 x 150	1-20	28	—	—	145	56	8	576	—	16
5000	LINEAR	122 x 163	1-20	40	—	—	199	107	8	858	—	12
7600	(L/LS) LINEAR	98 x 118	1-15	25	—	10 DUAL	138	26	4	384	139	—
8000	(H.V.) LINEAR	105 x 123	1-50	23	—	2 ZENER 28V	60	32	2	427	—	—

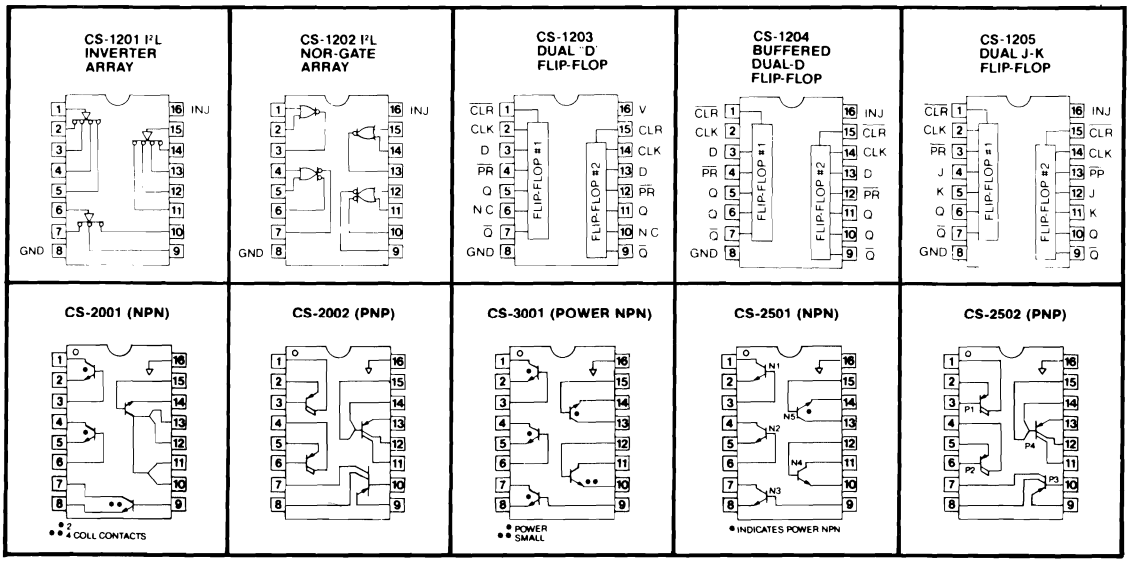
RESISTOR DETAIL
LINEAR SEMICUSTOM ARRAYS

RESISTOR TYPE & VALUE	GENESIS TYPE NUMBER													
	1100	1500	2200E	2500G	2800	3000F	3100	3200L	3500	3600	4000M	5000	7600	8000
DIFFUSED														
100Ω	—	—	—	—	—	8	12	12	—	16	—	14	—	—
135Ω	12	10	—	—	—	—	—	—	—	—	—	—	—	—
240Ω	—	—	10	27	27	37	42	42	20	68	60	64	—	41
270Ω	26	76	—	—	—	—	—	—	—	—	—	—	118	—
450Ω	—	—	46	71	72	122	20	99	60	139	188	228	—	114
600Ω	103	94	—	—	—	—	—	—	—	—	—	—	102	—
900Ω	—	—	55	69	69	122	10	89	64	121	140	268	102	268
1.2KΩ	105	146	—	—	—	—	—	—	—	—	—	—	49	—
1.8KΩ	—	—	24	44	44	80	2	63	36	82	104	152	—	142
2.4KΩ	55	70	—	—	—	—	—	—	—	—	—	—	51	—
3.6KΩ	—	—	20	28	28	52	—	42	26	56	84	132	—	28
4.8KΩ	38	56	—	—	—	—	—	—	—	—	—	—	52	—
ION-IMPLANT														
4KΩ	—	—	—	—	—	—	79	—	—	—	—	—	17	—
12KΩ	—	—	—	—	—	—	79	—	—	—	—	—	65	—
18KΩ	—	—	—	—	—	—	—	—	—	—	—	—	30	—
24KΩ	—	—	—	—	—	—	61	—	—	—	—	—	27	—
48KΩ	—	—	—	—	—	—	42	—	—	—	—	—	—	—
PINCH														
30KΩ	—	—	—	—	—	—	—	—	—	—	—	—	—	—
60KΩ	8	4	8	8	8	16	8	8	8	12	16	12	—	—

9

GENESIS CHIP	2200E, 2200EX, 2500G, 2500GX, 2800, 2800X, 3000F, 3000FX, 3100, 3100X, 3200L, 3200LX, 3500, 3500X, 3600, 3600X, 4000, 4000MX, 5000, 5000X						1100		1400		1500		ALL	
TRANSISTORS	SMALL NPN		MEDIUM NPN		LARGE NPN		SMALL NPN		MEDIUM NPN		LARGE NPN		LATERAL PNP	
	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS
V_{CEO}@10μA V	25	20	25	20	25	20	15	12	15	12	15	12	—	+Vcc
I_{CEO}@10V μA	—	.001	—	.005	—	.01	—	.002	—	.01	—	.02	—	002
V_{EBO}@10μA V	6.8	6.3-7.3	6.8	6.3-7.3	6.8	6.3-7.3	6.8	6.3-7.3	6.8	6.3-7.3	6.8	6.3-7.3	—	+Vcc
h_{FE}@10μA, 5V	150	80-400	—	—	—	—	150	80-400	—	—	—	—	40	20-200
h_{FE}@100μA, 5V	170	80-500	—	—	—	—	170	80-500	—	—	—	—	30	15-130
h_{FE}@10mA, 5V	120	40-240	170	40-310	170	40-310	120	40-240	170	40-310	170	40-310	—	—
h_{FE}@100mA, 5V	—	—	150	30-250	150	40-250	—	—	150	30-250	150	40-250	—	—
R_{SAT}@10mA Ω	50	30-80	9	6-15	6	4-10	50	30-80	9	6-15	6	4-10	500 (@100μA)	
R_{SAT}@10mA Ω	25	20-60	6	3-10	4	2-6	25	20-60	6	3-10	4	2-6	—	—
R_{SAT}@100mA Ω	—	—	9	6-15	6	4-10	—	—	9	6-15	6	4-10	—	—
R_{SAT}@100mA Ω	—	—	6	3-10	4	2-6	—	—	6	3-10	4	2-6	—	—
f_T MHz	400	—	380	—	350	—	400	—	380	—	350	—	4	—
OPERATING CURRENT RANGE	0.1μA to 20mA		1μA to 100mA		1μA to 150mA		0.1μA to 20mA		1μA to 100mA		1μA to 150mA		0.1μA to 1mA	
OPERATING CURRENT RANGE	.1μA to 40mA		1μA to 200mA		1μA to 350mA		.1μA to 40mA		1μA to 200mA		1μA to 350mA		1μA to 1mA	

SELECTION GUIDE
BREADBOARD COMPONENTS



TYPE NUMBER	COMPONENT CONTENTS	CIRCUIT COMPATIBILITY
CS-1201	3 I²L INVERTERS	1100
CS-1202	4 I²L NOR GATES	1200
CS-1203	1 DUAL 'D' FLIP FLOP	
CS-1204	1 DUAL 'D' FLIP-FLOP (B)	1400
CS-1205	1 DUAL 'J-K' FLIP-FLOP	
CS-2001	4 SMALL NPN	2000E
CS-2002	4 LATERAL PNP	2000EX
CS-3001	1 SMALL NPN 4 POWER NPN	3000F 3000FX
CS-2501	4 SMALL NPN 1 POWER NPN	2500G, 2800, 3100, 3200L, 3500,3600, 4000M
CS-2502	4 LATERAL PNP	(PLUS "X" VERSIONS)

9

CSC™ CHERRY SEMICONDUCTOR

GENESIS™

LINEAR DIGITAL SEMICUSTOM ARRAYS

GENERAL

Integrated Injection Logic (I^2L) technology extends the capabilities of semicustom design to high complexity digital or combined analog/digital systems. CSC has made this possible by the development of a family of I^2L Gate Arrays which combine a large number of I^2L gates and Schottky-bipolar transistors on the same chip. CSC's I^2L semicustom program utilizes partially fabricated silicon wafers which are then "customized" by the application of special mask patterns.

CSC's digital arrays utilize bipolar input//output (I/O) interface circuitry on the same chip, along with the high-density I^2L logic. Thus, outwardly the I^2L semicustom chip looks and performs exactly as a bipolar L SI chip, which can readily interface with TTL or MOS level signals. In other words, these GENESIS gate-arrays combine the high functional density advantages of I^2Ltechnology with the interface and load-drive capability of the bipolar circuitry on the same IC. This feature makes it very convenient to "retrofit" I^2L LSI designs into existing MOS or TTL type logic systems.

ACHIEVING HIGH COMPLEXITY

Traditionally, the application of semicustom design technology to complex digital systems has been somewhat limited due to one key factor: to be economically feasible, a complex digital LSI circuit must achieve a high functional density on the chip (i.e., high-gate count per unit chip area). This requirement is not compatible with the random interconnection concept which is key to the semicustom design technique. The GENESIS approach to this problem overcomes this limitation and achieves packing densities approaching those of full custom digital LSI layout while still maintaining the low-cost and quick turn-around of semicustom IC design. This is achieved by making use of unique layout and interconnection properties of I^2L gates, and by extending the customizing steps to other mask layers, as well as the metal interconnection pattern.

CSC's arrays are customized by not one but three mask layers:

1. A custom diffusion pattern to define gate outputs and custom "underpasses" for connection.
2. A custom "contact" mask which opens contact windows or "activates" only those devices actually used in the design.
3. A custom metal interconnection mask which interconnects all the "activated" devices.

FULLY-AUTOMATED MASK GENERATION

CSC has developed a fully-automated mask-generation technique which allows all three custom mask layers to be generated simultaneously; directly from a customer's pencil layout on the GENESIS worksheet. This unique mask generation technique and the three mask customizing method are the heart of CSC's I^2L semicustom program. In this manner, one is able to combine low-cost quick turn-around capabilities of semicustom designs with the high functional density of I^2L technology, and make very efficient use of the chip area.

WHEN TO USE DIGITAL SEMICUSTOM

The key application of I^2L semicustom design is to replace complex blocks of random-logic functions with a single monolithic chip. An entire digital sub-system comprised of many SSI or MSI chips, or discrete components can be put on a single GENESIS I^2L Chip, thus providing significant cost and space savings and greatly improving system reliability. The availability of bipolar input-output interface circuitry on the same chip along with the high-density I^2L logic makes it very convenient to retrofit I^2L designs into existing MOS or TTL logic systems. Therefore semicustom I^2L LSI designs provide cost-effective solutions for complex custom LSI requirements.

FEATURES OF I^2L TECHNOLOGY

Integrated Injection Logic (I^2L) is one of the most significant advances in the area of monolithic LSI technology. Compared to other technologics, I^2L offers the following unique advantages.

High Functional Density: I^2L logic gates offer much smaller size than other digital bipolar techniques. Thus a much higher degree of logic complexity or functional density can be achieved on a given IC chip.

Easy to Interconnect: Unique structure and geometry of I^2L gates make them ideal for semicustom design. An entire array of gates can be easily customized and interconnected with only three masks, without sacrificing high functional density.

Bipolar Compatible Processing: I^2L is a direct derivative of conventional bipolar IC technology. Therefore, one can combine bipolar devices on the same chip as I^2L gates. This feature has the following key advantages:

- Input-output sections of I^2L chips can be made bipolar. Thus, they can readily interface with existing logic families or retrofit into existing systems.

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

FEATURES OF I²L TECHNOLOGY CONTINUED

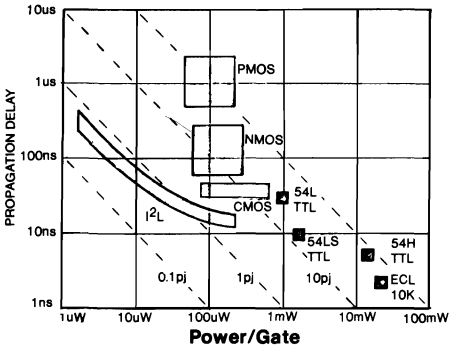
- Analog and digital functions can be combined on the same chip. One of CSC's GENESIS Chips, the 1400 is specifically designed for such an application.

Low-Voltage Operation: I²L gates can operate with supply voltages as low as 1 volt, and require only a single power supply.

Low-Current and Low-Power Operation: I²L can operate with current levels in the nano-Ampere range. This feature, along with its low-voltage operation makes it ideal for applications in low-power, battery operated systems.

Higher Reliability than MOS: Since I²L gates have the same basic features of bipolar transistors, they are not subject to electrostatic burn-out problems associated with MOS transistors, and do not require special handling precautions.

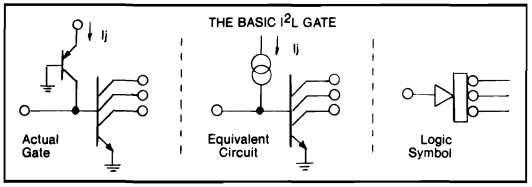
Wide Operating Temperature: I²L gates are not as affected by leakage currents as their MOS counterparts. Thus they can be made to operate over the full military temperature range.



Comparison Of Speed/Power Capabilities Of Common Logic Families

The BASIC I²L GATE

The I²L logic technology is derived from the basic single-input, multiple-output inverter circuit shown below. The logic functions are ferformed in a manner similar to the case of conventional "open-collector" logic i.e., the outputs of various gates are interconnected together, in a wired-AND configuration. Most terminals of the I²L gate share the same semiconductor region (for example, the collector of the PNP is the same as the base of the NPN; and the emitter of the NPN is the same as the base of the PNP). This leads to a very compact device structure which occupies a very small chip area. As a result, the functional density of I²L gates on a chip is comparable to that of MOS gates, and is approximately 5 times higher than conventional TTL logic.



LOGIC CONVERSION TO I²L GATES

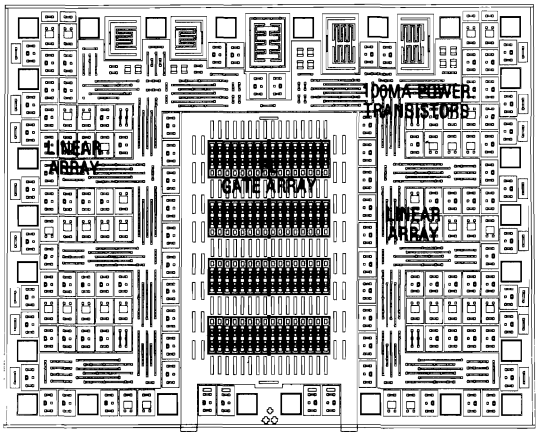
Converting conventional logic diagrams from their NAND/NOR gate equivalents to I²L gates is a simple and straightforward procedure. CSC has developed a large "Library" of I²L logic blocks corresponding to popular logic functions, such as decoders, flip-flops and counters, which greatly simplifies this conversion process.

DESIGNING WITH I²L GENESIS CHIPS

CSC currently has threee arrays in production that combine linear and I²L digital capability, the 1100, 1400 and 1500.

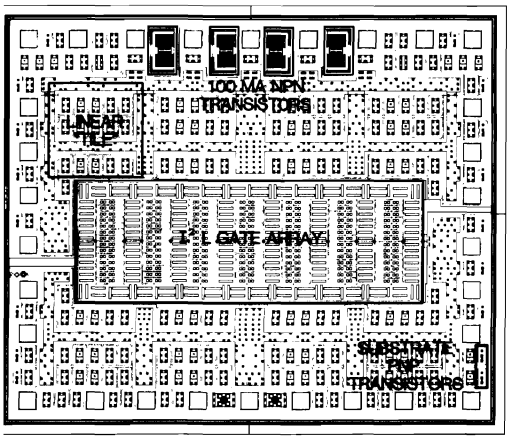
These GENESIS Chips are fabricated with the same manufacturing process. They differ only in their architecture and the number of components. All of these chips are especially designed for CSC's unique multi-mask customization process, using fully-automated mask generation techniques.

BASIC LAYOUT ~ 1100



9

BASIC LAYOUT ~ 1500



GENESIS 1400

The 1400 Chip is designed primarily for applications requiring a combination of analog and digital functions on the same chip. Thus, it is made up of both a linear and a digital section. The digital section of the chip contains 256 5-output I²L gates and 18 Schottky-bipolar I/O interface sections. The linear section of the chip is made up of an array of NPN and PNP transistors and resistors, and is similar to CSC's linear arrays.

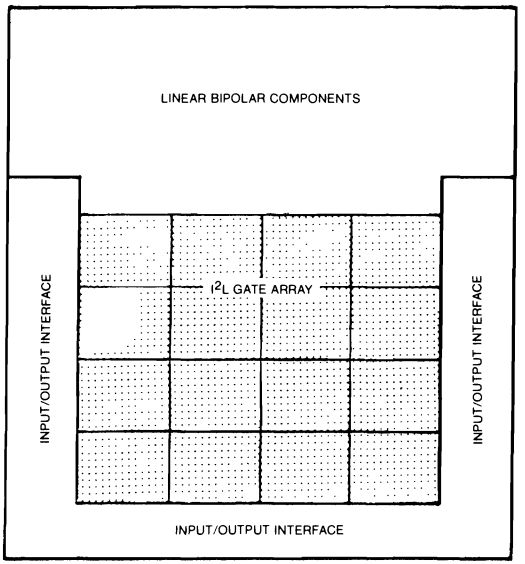
Compared to conventional linear arrays, the GENESIS 1400 offers superior layout flexibility and component utilization. The multi-mask customization process required to "personalize" the digital section provides several unique advantages in the linear section. While the location of transistors is pre-defined, their designation as NPN or PNP is not; thus the mix can be tailored to meet the specific requirements of a circuit. Additionally the transistors can be rotated to enhance layout flexibility. Transistors can be selectively omitted and replaced with multi-conductor underpasses.

In the resistor field, the specific values and locations of resistances has not been pre-defined. Only the required resistors need be diffused, and they can be located to accomodate the layout. The value of resistors is established by specifying the length on a grid, and is continuously variable in steps of approximately 400 ohms, over the range of 600 ohms to over 40K ohms.

CONVENTIONAL LINEAR ARRAY VS GENESIS 1400

	CONVENTIONAL	1400
TRANSISTORS:		
Location	Fixed	**Fixed**
Designation	Fixed	**Selectable**
Orientation	Fixed	**Selectable**
Mix	Fixed	**Variable**
Multi-emitter	No	**Yes**
Special geometries	No	**Available**
RESISTCRS:		
Value	Fixed	**Variable**
Mix	Fixed	**Variable**
Location	Fixed	**Variable**
Orientation	Fixed	**Selectable**

BASIC LAYOUT ~ 1400



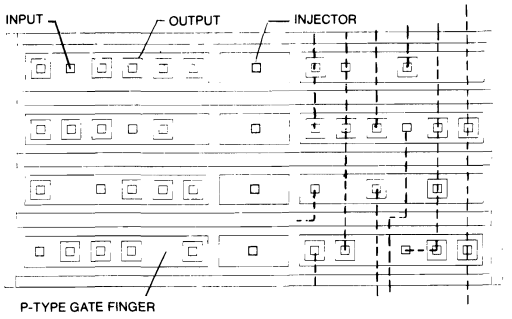
COMPONENT UTILIZATION

The multi-mask customizing technique used in CSC's I²L Chips makes them very efficient for both ease of logic layout and component utilization. One of the three customizing mask steps is a "custom diffustion" step which allows one to place low-resistance underpasses selectively on the chip. This technique provides the designer with virtually two layers of interconnection on the chip, thus greatly simplifying the logic layout, and improving the component utilization. Normally, in the case of random combinational logic, one can utilize 60% to 80% of the total gates available on a given I²L Chip. In the case of sequential and repetitive logic circuits, the gate utilization is normally in the 80% to 90% range.

The I²L GATE ARRAY SECTION

This section of the I²L GENESIS chip is made up of logic "cells" which contain a number of multiple-output I²L inverters, grouped together. The figure on page 4 shows the typical layout of such a cell made up of eight multiple output inverters which share a common set of four injectors. The basic gate cells forming the I²L gate array are made up of P-type injectors and P-type gate fingers which serve as the base regions of the I²L gates. The six possible sites on each gate finger can be programmed as either gate input, output or left unused. The particular use of these sites as an input or an output is determined by two custom masks: an N-type collector diffusion mask which defines the locations of outputs, and a custom contact mask which opens the appropriate input and output contact. Finally, a third custom mask is applied to form the metal interconnections between the gates and the gate cells. The custom N-type diffusion step, which determines the locations of gate

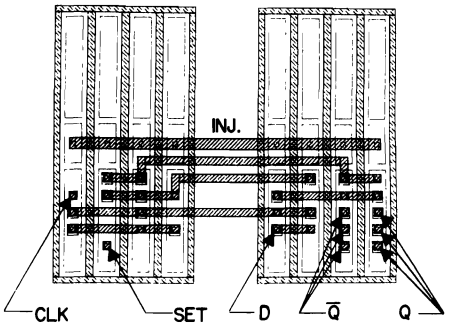
outputs, is also used for forming low-resistivity underpasses between the gate cells. The area between each of the gate cells can accommodate two or three parallel underpasses in the horizontal and the vertical direction,



Typical Layout of I²L Cell (8 Gates)

respectively. Since the N-type diffusion which forms these underpasses is part of the customizing step, the location and the length of each underpass can be chosen to fit a given interconnection requirement. This method provides the designer with virtually all the advantages and capabilities of multi-layer interconnection paths on the surface of the chip; and allows approximately 80% of the gates on the chip to be utilized in a typical logic layout.

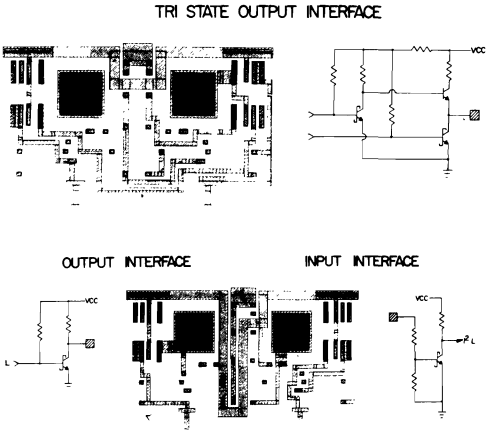
The custom logic interconnections can be easily laid out in pencil on a layout sheet by simply interconnecting the desired gate sites with a pencil line and appropriately defining the function of the site as an input, output, injector contact or an underpass.



A "D" Flip-Flop With Set Input As An Example Of A Basic Layout After Customizing.

BIPOLAR INPUT/OUTPUT INTERFACE SECTION

The bipolar input/output interface sections of the GENESIS I²L arrays are located along the periphery of the chips. The topography of typical I/O cells is shown below. Each I/O cell is designed to be either an "input" or an "output" interface, depending on the choice of the metal inerconnection pattern applied to the cell. Furthermore, two adjacent cells can be combined to provide a tri-state type output buffer. Some of the basic input and output circuit configurations available from the I/O interface are shown below. In the case of a tri-state output configuration, one would also utilize several gates from the I²L logic section, to perform the necessary gating functions.



Typical Bipolar Input/Output Interface Circuits Available From I/O Interface Cell

Each input/output interface cell contains one bonding-pad, several resistors of varying values, a clamp-diode to substrate and two NPN transistors with optional Schottky-diode clamps. One NPN transistor is capable of sinking 5mA of current with Schottky-diode clamps, and 10mA of current without Schottky-diode clamps, at a saturation voltage of <0.5V. The breakdown-voltage of the bipolar I/O section is 12V.

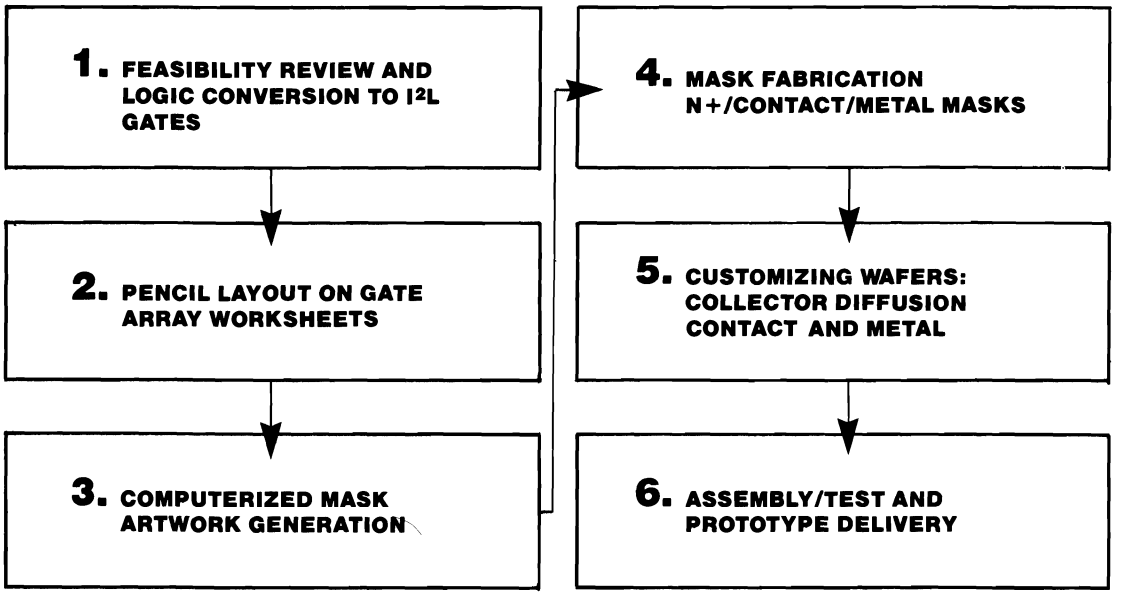
DIGITAL SEMICUSTOM DESIGN CYCLE

The digital semicustom LSI design program using CSC's I²L arrays provides maximum versatility and flexibility, to suit varying customer needs and capabilities. The flow-chart below gives the outline and the sequence of six basic steps associated with a typical I²L semicustom program.

In many cases, the first two steps indicated in the flow-chart can be done by the customer, in consultation with CSC.

9

SIX BASIC STEPS OF SEMICUSTOM I^2L DEVELOPMENT



Step 1: Feasibility Review And Logic Conversion To I^2L Gates

Starting with the customer's logic diagram (preferably reduced to flip-flops and gates) the first step is a detailed review of the system requirements with regards to the overall gate count, I/O requirements, operating speeds, etc., to assure feasibility of integration, and to choose the most economical gate array chip to be used. If the results of this review indicate feasibility, the next step is to convert the logic diagram into I^2L gates. At this state, a computer simulation of the logic diagram may also be performed, if deemed necessary.

Step 2: Pencil Layout On Gate Array Worksheets

Once the logic diagram is converted to I^2L gates, the next step will be to make a pencil layout of the circuit on the appropriate array worksheet. This pencil layout is done on a blank worksheet where the gate input and output locations are shown as target dots. During the layout, an appropriate symbol is placed over the corresponding dot on the gate outline and the interconnections and the underpasses between the gates are indicated by pencil lines and with appropriate symbols. In this layout, the bipolar I/O cells do not need to be internally connected. Since these cells are standardized, it is only necessary for the designer to specify if a particular I/O cell is to be used as an input or an output.

Step 3: Computerized Mask Artwork Generation

Using a specially developed computerized mask generation technique, the three layers of necessary custom IC tooling can be automatically generated by a single "digitizing" step from the pencil layout. This simultaneous and automated generation of the three custom mask layers greatly reduces the tooling cost and turnaround time, and avoids mask errors.

Step 4: Mask Fabrication N+/Contact/Metal Masks

The photographic tooling plates, or "masks," are fabricated by a pattern-generation technique from the digitized coordinate information stored in the computer.

Step 5: Customizing Wafers: Collector Diffusion Contact And Metal

The prefabricated I^2L wafers containing the P-type base diffusion and the gate "fingers" are customized into completed monolithic LSI chips using the custom IC tooling generated in Steps 3 and 4.

Step 6: Assembly/Test And Prototype Delivery

The completed monolithic chips are first evaluated on the finished IC wafer, and later assembled, electrically tested and delivered as the completed prototypes. The amount of electrical testing done on the initial prototypes depends on the customer's specific needs and requirements.

CHERRY SEMICONDUCTOR

GENESIS™

LINEAR SEMI CUSTOM ARRAYS

SEMICUSTOM CONCEPT

GENESIS linear semicustom ICs are uncommitted arrays of transistors and diffused resistors fabricated on a single monolithic silicon chip. Wafers are held in inventory with over 80% of the process steps completed. By application of a unique interconnect (metalization pattern, the array is converted into a "custom" integrated circuit.

GENESIS semicustom ICs offer the advantages of proprietary design at a fraction of the development time and tooling cost of a "full-custom" program. Semicustom programs are ideally suited to applications where moderate production volumes are required and short prototype lead time is important.

Should future production levels increase, GENESIS ICs can be converted to full custom versions, thus assuring the lowest possible unit cost. Since the design is already proven, the conversion is essentially risk free. CSC's "guaranteed investment" program provides additional savings, since a portion of the GENESIS development charges are credited against the full custom tooling.

GENESIS semicustom ICs are diffused, manufactured, and tested in CSC's own facility, where we routinely support production volume from a few hundred to hundreds of thousands of circuits per month.

GENESIS LINEAR CIRCUITS

A broad selection of GENESIS linear arrays is available with die areas from 5800 to 20,000 square mils, and integrated component counts ranging from 200 to over 1200.

Included in the product line are two unique special purpose ICs. The GENESIS 2800 is available in ***Flip-Chip*** form, for direct solder reflow mounting. The GENESIS 3500 is designed specifically for optoelectronic applications, and features an integrated on-chip photodetector. These two devices are fully supported by our in-house specialized diffusion, packaging, and testing capabilities. The GENESIS 2800 and 3500 are a natural outgrowth of CSC's years of experience supplying ICs in large production volumes to the hybrid and photographic industries, and their existence marks an extension of the spectrum of technology now available to semicustom users.

In addition to ***Flip-Chip***s and optoelectronic circuits, CSC offers several unique options and services to further enhance the scope of GENESIS IC applications. These include the extended performance option, active wafer trimming, and multichip assemblies.

GENESIS package options include, in addition to industry standard dual-in-line epoxy and ceramic outlines, a selection of surface mount and transparent molded assemblies.

DESIGN KIT ARRAYS are available to assist you in breadboarding a preliminary circuit. They contain appropriate quantities of linear array components that are matched to a specific Genesis™ semicustom circuit. Individual arrays are available for digital applications.

KIT NUMBER	ARRAY KIT CONTENTS					PRICE
	2001	2002	3001	2501	2502	$
K2000	10	5	1	—	—	25.00
K3000	25	12	2	—	—	60.00
K2001	10	—	—	—	—	18.00
K2002	—	10	—	—	—	18.00
K2500	—	—	—	10	5	25.00
K3200	—	—	—	25	12	60.00
K2501	—	—	—	10	—	19.00
K2502	—	—	—	—	10	19.00

SPECIAL FEATURES & PROGRAMS

Extended Performance: By adding a collector diffusion option to the standard GENESIS linear process, several performance advantages are realized.

1) NPN transistor operating current range is extended by 50% to 100%, up to 400mA for the power devices.
2) NPN transistor saturation resistances are reduced by up to 50%, allowing high current loads to be driven with lower IC dissipation.
3) A thicker oxide is grown over the collector underpasses, allowing the circuit to withstand high voltage transients while eliminating the layout restrictions typically associated with collector underpass use.

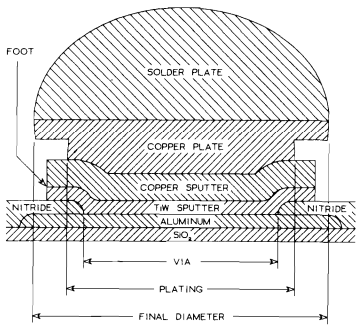
CAD Compatibility: These GENESIS arrays are designed topographically on a uniform grid to take maximum advantage of modern computer graphics techniques. This feature allows more rapid entry of designs into our computer aided layout and mask generation system, thereby reducing turnaround time for new designs. The CAD compatible GENESIS arrays also permit remote site layout entry direct to the computer, either at an authorized GENESIS Design Center or at the customer's own facility.

Optoelectronics: These GENESIS devices can be housed in a transparent epoxy package, along with a silicon photodetector. The result is an electrically and optically pre-tested semicustom optoelectronic component. CSC is equipped to completely design, fabricate, package, and test these assemblies in house.

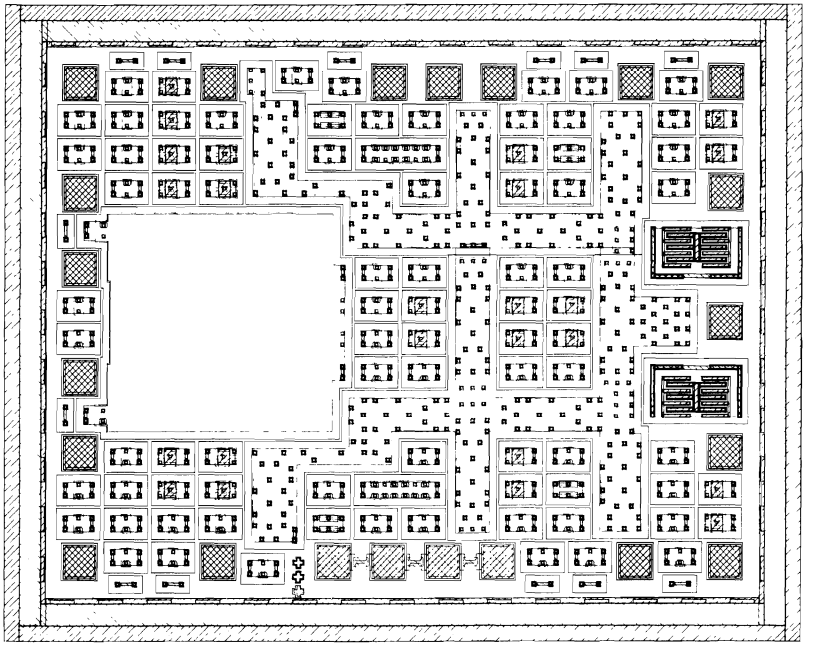
The GENESIS 3500 is designed specifically for optoelectronic applications, and offers the added convenience and economy of an on-chip photodetector. It is suited for a variety of optoelectronic applications requiring a light-sensitive function combined with additional signal processing capability. In addition to the built in photodetector, the 3500 contains 85 transistors and 214 resistors. allowing optoelectronic functions and systems to be implemented with a single component.

Flip-Chip* Technology:** The GENESIS 2800 is available as an unpackaged chip with tin/lead "solder bump" terminals, designed for direct solder-reflow bonding to hybrid substrates. Since wire bonds are eliminated, GENESIS ***Flip-Chips offer enhanced reliability and lower costs in the manufacture of hybrid assemblies. ***Flip-Chip***s are a preferred technology for such critical applications as military and underhood automotive electronics.

The GENESIS 2800 extends, for the first time, the advantages of solder bump technology to users of semicustom ICs. The 16 bumps of the 2800 can all be attached in a single solder reflow operation, along with chip capacitors and other hybrid components.



METALLURGY OF SOLDER BUMPS



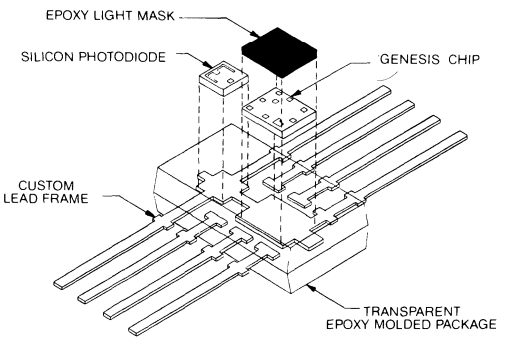
GENESIS™ 3500 OPTOELECTRONIC CHIP

Active Trim: All GENESIS arrays are designed to allow limited adjustment of one or more key parameters at wafer probe. This feature makes feasible circuit performance characteristics not usually attainable within the limitations of monolithic technology.

In the case of the GENESIS 3500 optoelectronic circuit, CSC can even actively trim light-dependent characteristics.

Multi-Chip Assemblies: Certain GENESIS chips can be combined with a second chip in a modified package to form unique, powerful components. Examples include GENESIS chips packaged with discrete power transistor chips, photosensors, temperature sensing chips, and LEDs.

KIT DESIGNATION	ARRAY KIT CONTENTS 2001	2002	3001	2501	2502	PRICE $
K2000	10	5	1	–	–	25 00
K3000	25	12	2	–	–	60 00
K2001	10	–	–	–	–	18 00
K2002	–	10	–	–	–	18 00
K2500	–	–	–	10	5	25 00
K3200	–	–	–	25	12	60 00
K2501	–	–	–	10	–	19 00
K2502	–	–	–	–	10	19 00



EXAMPLE OF MULTI-CHIP ASSEMBLY

TEST CAPABILITIES

CSC has extensive and sophisticated in-house test facilities for all products. GENESIS IC testing is performed on advanced computer controlled test systems. All production devices are 100% functionally and parametrically evaluated, both at the finished wafer level, and in packaged form.

GENESIS™ TEST CAPABILITIES	WAFER PROBE	PACKAGED IC
DC EVALUATION	●	●
AC EVALUATION	●	●
HI-SPEED LOGIC SIMULATION	●	●
ACTIVE TRIM	●	
HIGH-LOW TEMPERATURE TEST		●
PROGRAMMED ILLUMINATION*	●	●
AUTOMATIC PACKAGE HANDLING		●

*OPTOELECTRONIC DEVICES

DESIGN KIT ARRAYS

TYPE NUMBER	ARRAY CONTENT	CIRCUIT COMPATIBILITY
CS2001 CS2002	4 small NPN 4 lateral PNP	2000E 2000EX 3000F
CS3001	1 small NPN 4 power NPN	3000FX
CS2501	4 small NPN 1 power NPN	2500G/GX 2800/X 3200L/LX
CS2502	4 lateral PNP	3500/X 4000M/MX

Designs are usually developed with either discrete components or transistor arrays. For those customers doing their own design, we recommend standard carbon film resistors and GENESIS monolithic breadboard arrays. These arrays are made directly from the appropriate GENESIS wafer and will assure the most accurate simulation of the finished IC characteristics.

CUSTOMER-VENDOR INTERFACE

CSC provides one of the broadest programs of customer coverage in the industry. In addition to factory sales, applications, and engineering contacts, we are accessible through authorized regional GENESIS Design Consultants, and a world-wide network of sales representatives.

We welcome direct customer contact, and will quickly put you in touch with the person or department best able to answer your questions. Sales information, literature requests, applications assistance, and other inputs are routinely handled on a direct basis.

Our world-wide network of Sales Representatives can provide service at the local level, and are usually your most convenient contact for initial inputs, and for week-to-week interface with your requirements or business activity.

The GENESIS Design Consultants, located regionally in the U.S.A. and in Europe are equipped to provide a number of important services. These include circuit design, applications assistance, CAD interface, test definition, breadboarding, and prototype evaluation.

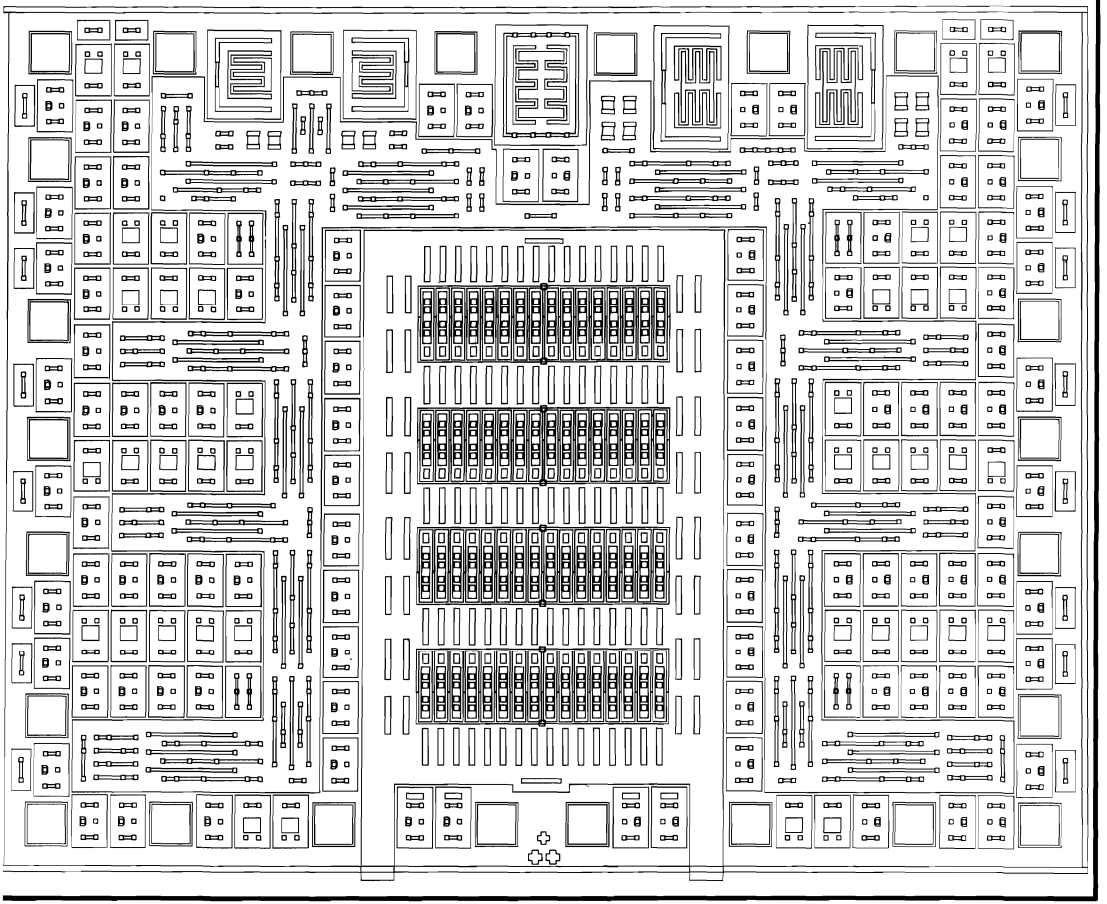
CHERRY SEMICONDUCTOR

I²L DIGITAL and LINEAR ARRAY

GENESIS™ 1100 SEMI-CUSTOM IC

The GENESIS 1100 is a powerful semicustom array for the simultaneous integration of standard linear and digital functions without performance compromises. It is a versatile bipolar linear array to which has been added a cluster of 64 Integrated-injection logic gates. The gates are speed-power programmable over a range of 100nA to 200μA, with corresponding propogation delays of 7μs to 50ns. Special components include Schottky-clamped NPN transistors for high speed logic interfaces, and power transistors with 400mA capability.

- CHIP SIZE: 98 x 124 mils
- BONDING PADS: 26
- MAX OPERATING VOLTAGE: 12V
- I²L GATES: 64
- MAX TOGGLE FREQUENCY: 2MHz
- NPN TRANSISTORS: 102
- PNP TRANSISTORS: 41
- RESISTORS — BASE: 339
  — PINCH: 8



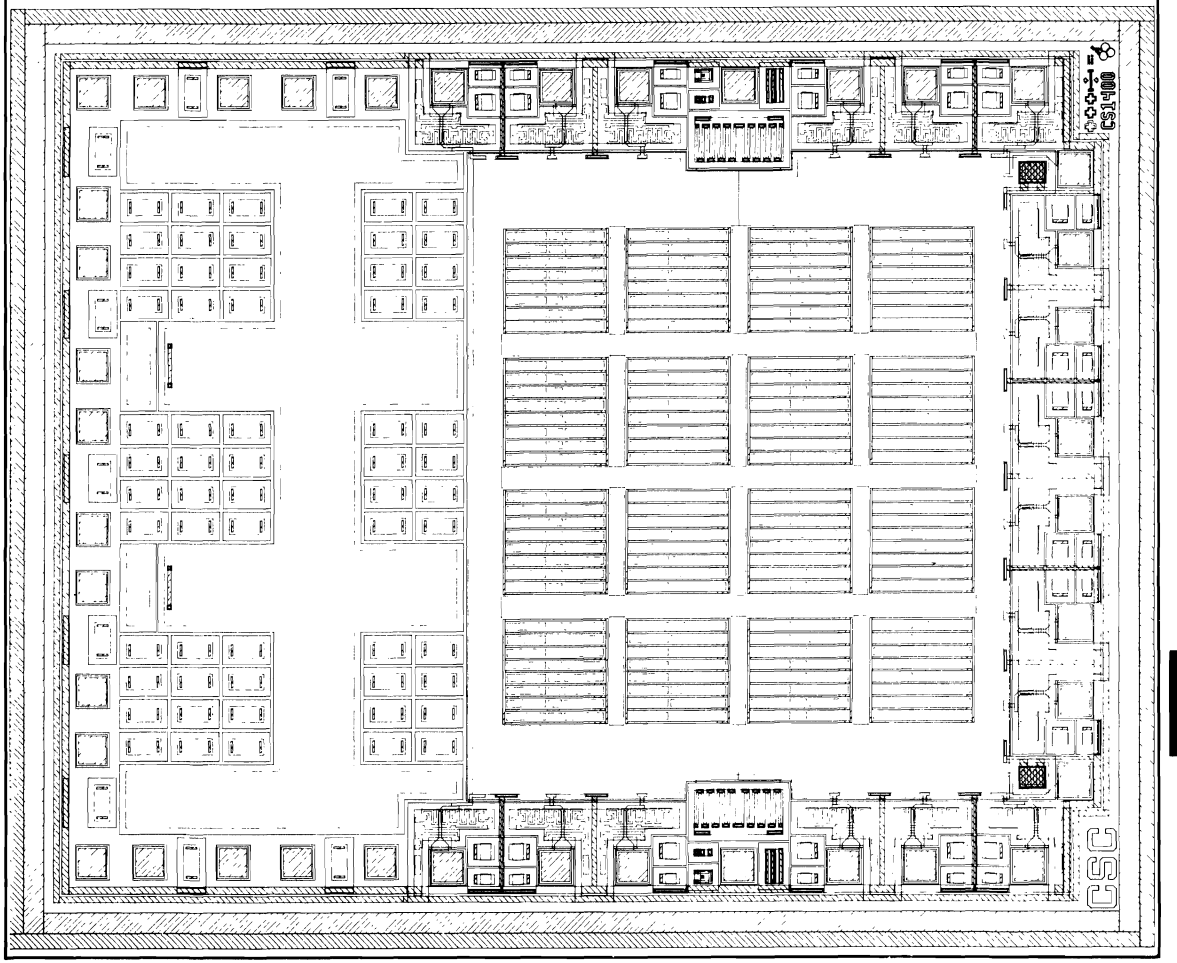
CHERRY SEMICONDUCTOR

I²L DIGITAL and LINEAR ARRAY

GENESIS™ 1400 SEMI-CUSTOM IC

- CHIP SIZE: 119 x 148 mils
- BONDING PADS: 40
- MAX OPERATING VOLTAGE: 12V
- I²L GATES: 256
- I/O INTERFACES: 18
- BIAS SECTION—
  NPN XSTRS: 4
  RESISTORS: 34
- MAX TOGGLE FREQUENCY: 2MHz
- LINEAR SECTION—
  NPN/PNP XSTRS: 69*
  RESISTORS: 200
- PACKAGES AVAILABLE:
  PLASTIC DIP 16-18-20-22-24-28-40
  S-B CERAMIC 16-18-22-24-28-40

*TOTAL OF NPN & PNP TRANSISTORS CAN NOT EXCEED 69 — MIX IS SELECTABLE



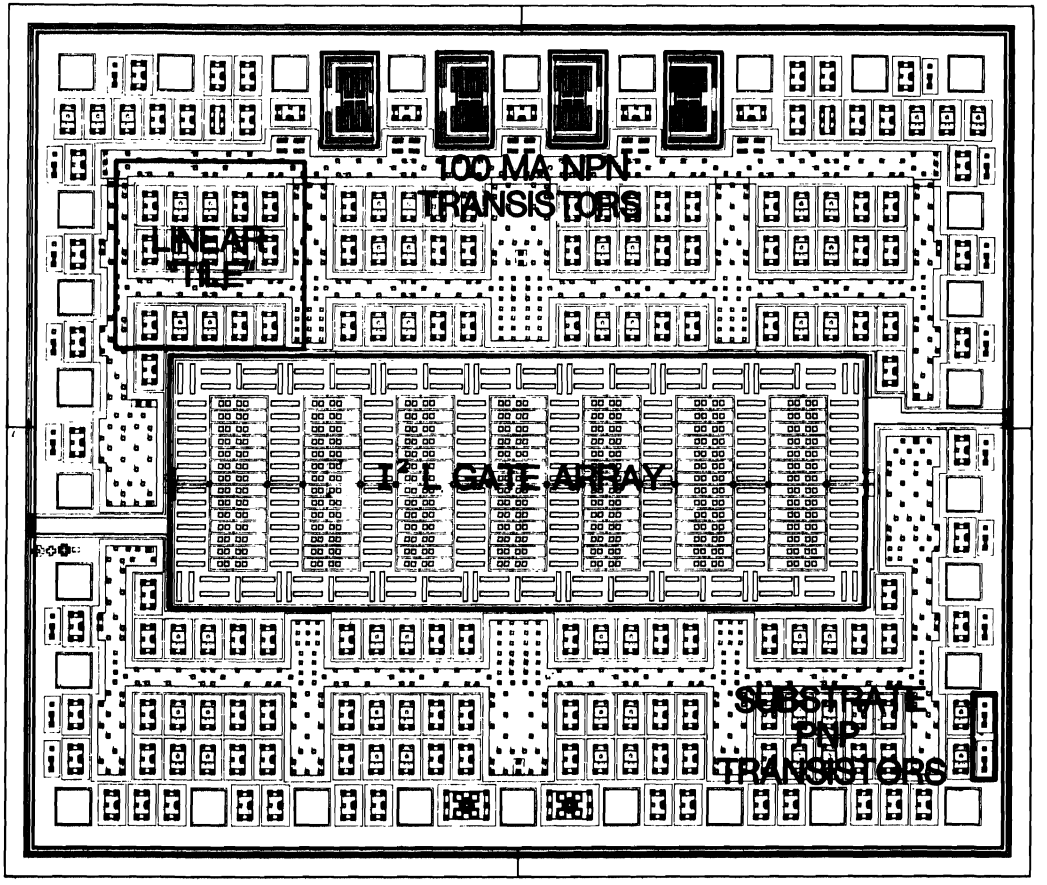
CHERRY SEMICONDUCTOR

I²L DIGITAL and LINEAR ARRAY

GENESIS™ 1500 SEMICUSTOM IC

Intended for single chip integration of complete systems, the GENESIS™ 1500 array provides a combination of digital and linear elements in the form of I²L gates and bipolar components. Included on the chip are 98 gates, 126 NPN transistors, 72 PNP transistors, 462 diffused base resistors (total resistance — 827KΩ) and 2 pinch resistors. The I²L devices are speed-power programmable and can be operated at currents as low as 0.1 microamp per gate. Supply voltage range is 1 to 12 volts

- TOTAL COMPONENTS: 760
- CHIP SIZE (mils): 123 x 140
- BONDING PADS: 30
- OPERATING VOLTAGE: 1V-12V
- I²L GATES: 98
- MAX TOGGLE FREQUENCY: 2 MHz
- NPN TRANSISTORS: 122 SMALL, 4 POWER
- PNP TRANSISTORS: 56 LATERAL, 16 SUBSTRATE
- RESISTORS — 4.8K (56) 600Ω (95)
  2.4K (70) 270Ω (84)
  1.2K (147) 135Ω (10)
  60K Dual Pinch (2)



CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY

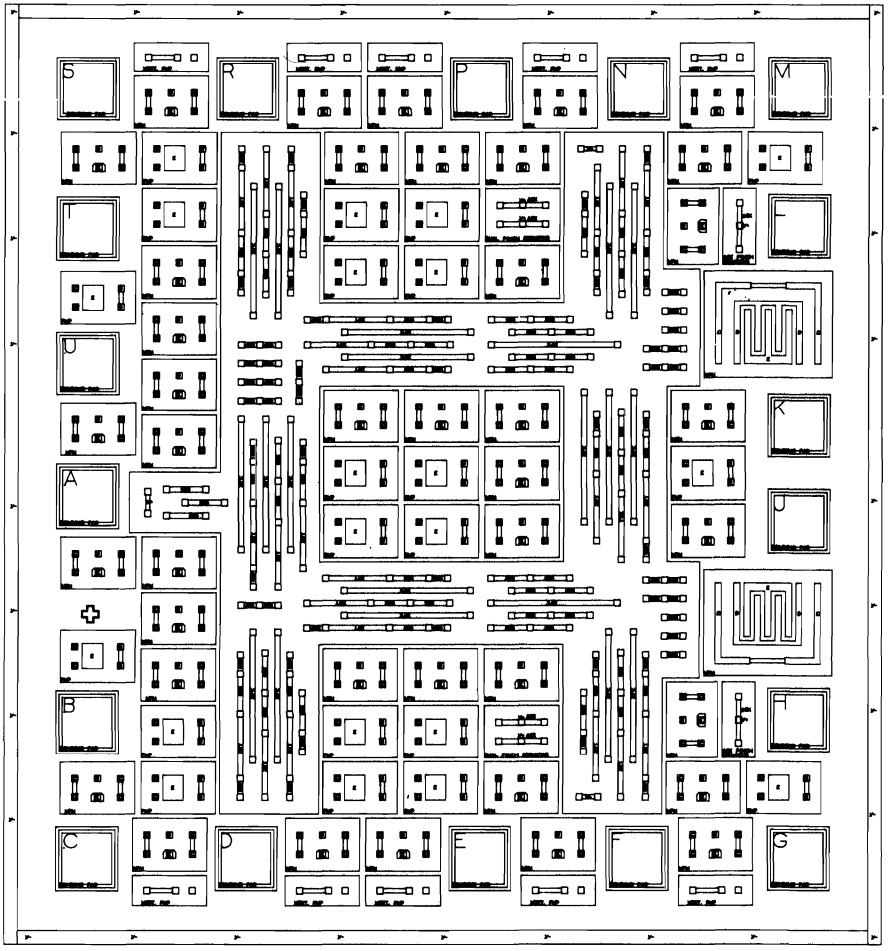
GENESIS™ 2200E, 2200EX SEMI-CUSTOM IC

The GENESIS™ 2200E and 2200EX are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. A unique metal interconnect mask is used to define the finished custom IC. The 2200EX is an extended performance version that doubles the useful operating current range of the NPN transistors.

- TOTAL COMPONENTS: 232
- CHIP SIZE (mils): 78 x 74
- BOND PADS: 18
- TRANSISTORS:
  - SMALL NPN 40
  - MEDIUM NPN 2
  - LATERAL PNP 21
  - SUBSTRATE PNP.....10

- RESISTORS:

3.6K	20
1.8K	24
900 ohms	55
450 ohms	46
200 ohms	10
Total resistance	187.4K
60K pinch	4



9

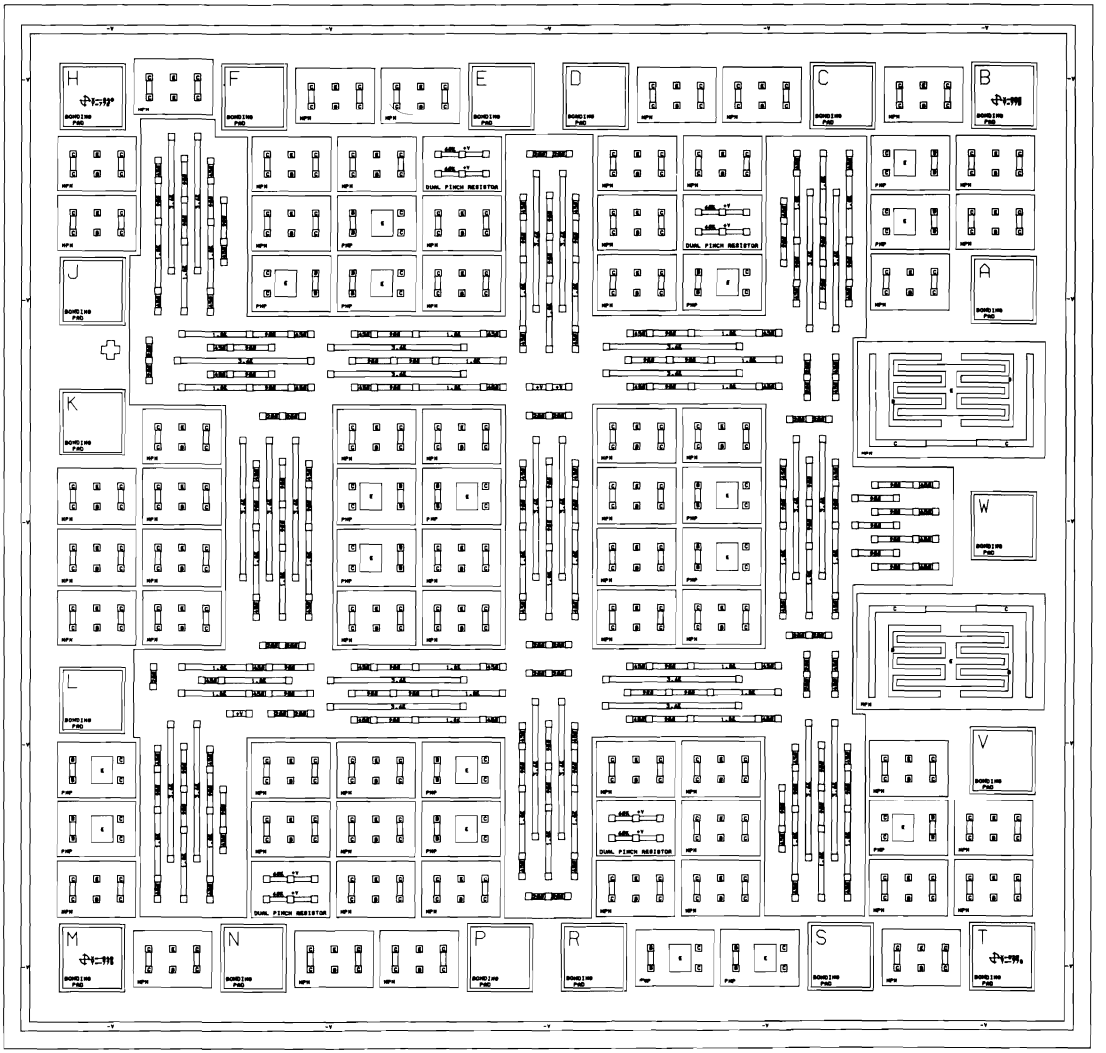
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY

GENESIS™ 2500G, 2500GX SEMI-CUSTOM IC

The Genesis 2500G and 2500GX are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. A unique metal interconnect mask is used to define the finished custom IC. The 2500GX is an extended performance version that doubles tne useful operating current range of the NPN transistors.

- TOTAL COMPONENTS: 325
- CHIP SIZE (mils): 75 x 79
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 18
- NPN TRANSISTORS: 58
- PNP TRANSISTORS: 18
- POWER NPN TRANSISTORS: 2
- TOTAL RESISTORS: 247



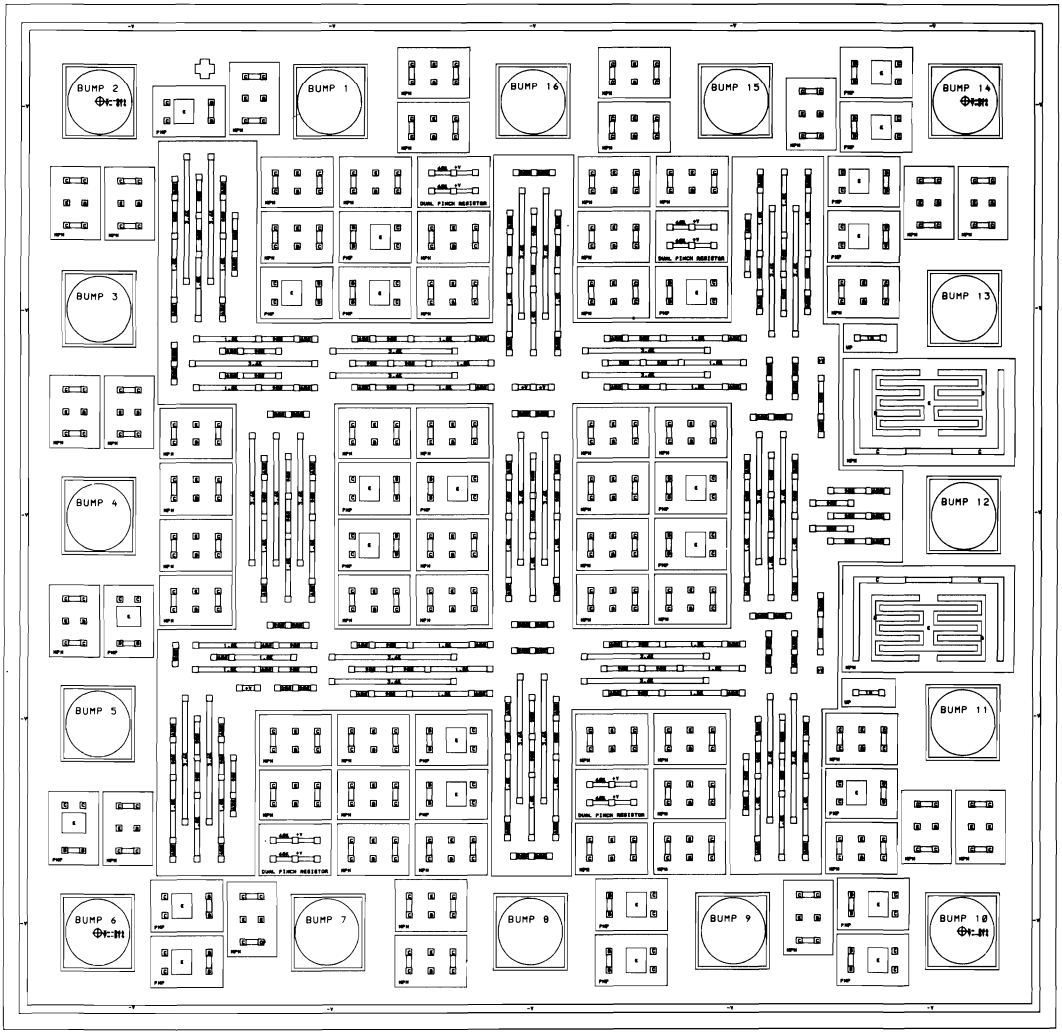
CHERRY SEMICONDUCTOR

LINEAR
BIPOLAR ARRAY
Flip-Chip

GENESIS™ 2800, 2800X SEMI-CUSTOM IC

The Genesis 2800 and 2800X are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. They feature controlled collapse solder bumps for reflow solder attachment to hybrid substrates. A unique metal interconnect mask is used to define the finished custom IC. The 2800X offers extended performance that doubles the useful current range of the NPN transistors.

- TOTAL COMPONENTS: 333
- CHIP SIZE (mils): 80 x 85
- MAX OPERATING VOLTAGE: 20V
- SOLDER BUMPS: 16
- NPN TRANSISTORS: 58
- PNP TRANSISTORS: 25
- POWER NPN TRANSISTORS: 2
- TOTAL RESISTORS: 248



9

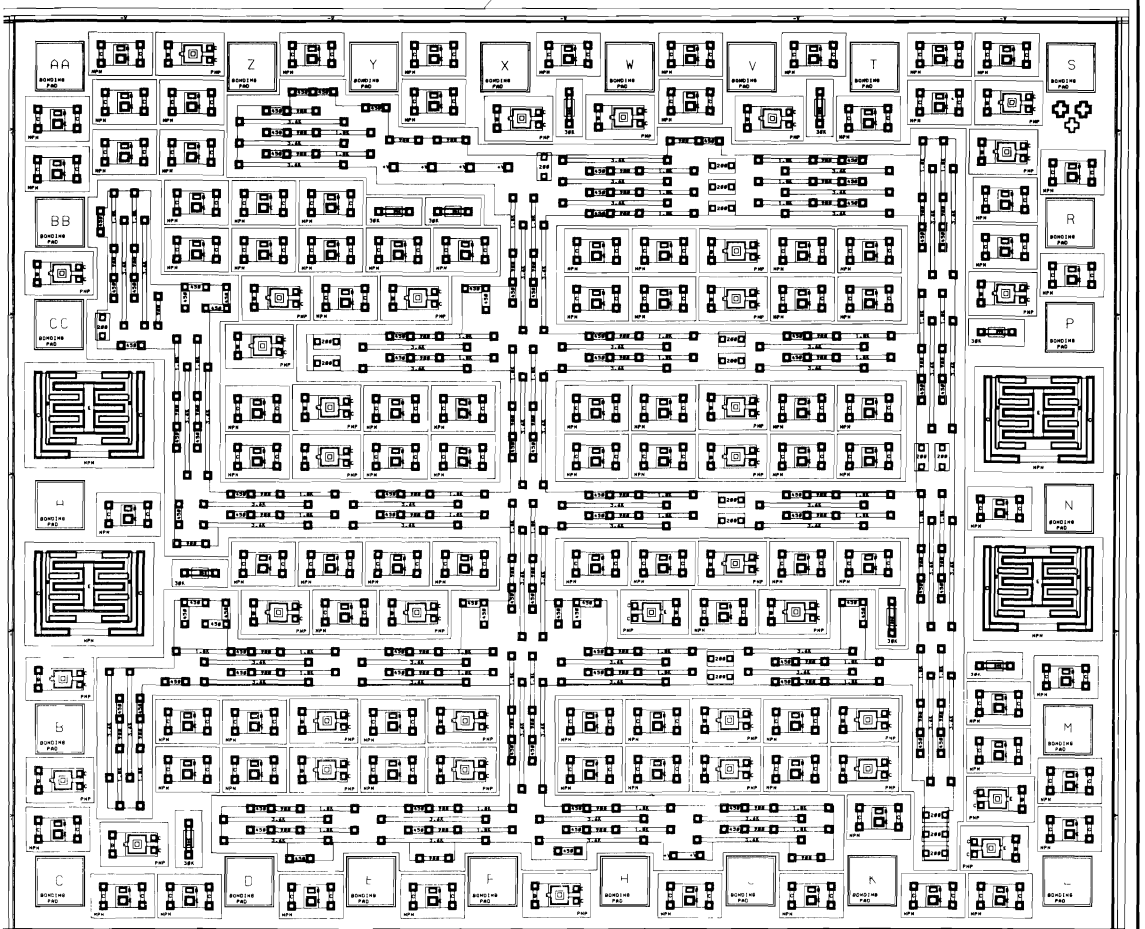
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY

GENESIS™ 3000F, 3000FX SEMI-CUSTOM IC

The Genesis 3000F and 3000FX are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. A unique metal interconnect mask is used to define the finished custom IC. The 3000FX is an extended performance version that doubles the useful operating current range of the NPN transistors.

- TOTAL COMPONENTS: 437
- CHIP SIZE (mils): 91 x 110
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 24
- NPN TRANSISTORS: 92
- PNP TRANSISTORS: 36
- POWER NPN TRANSISTORS: 4
- TOTAL RESISTORS: 305



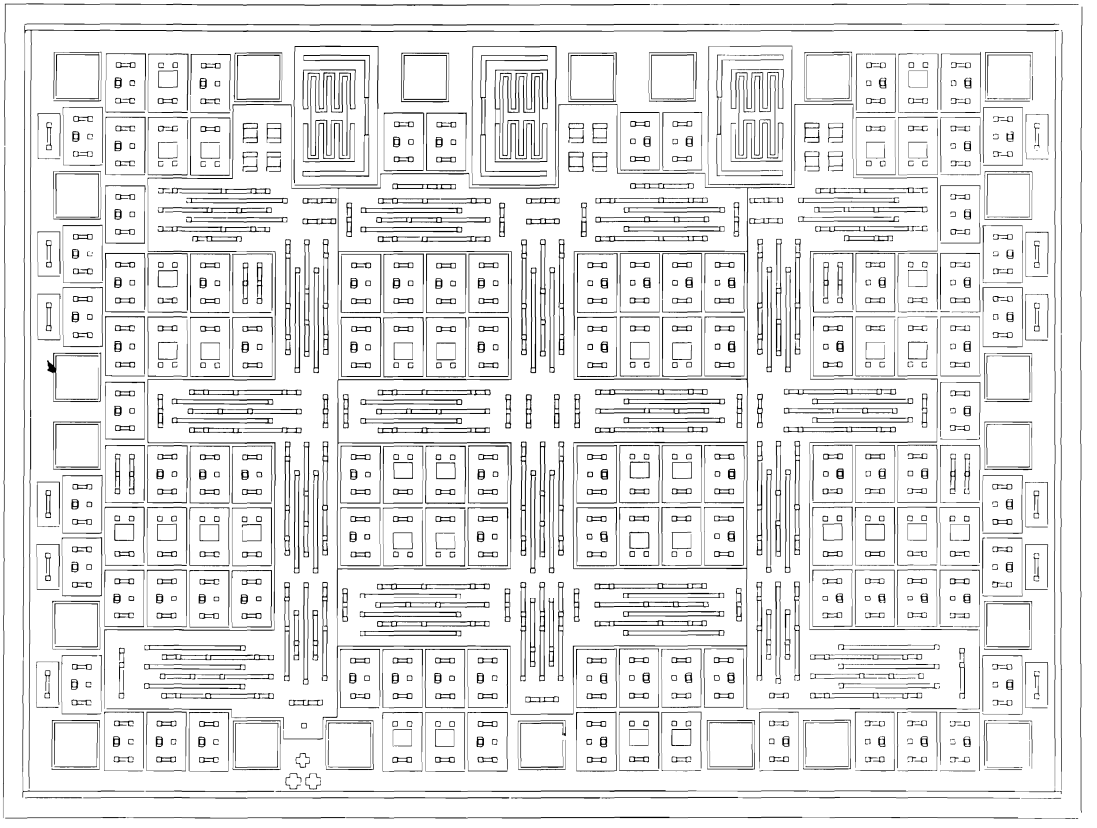
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY
(MICROPOWER)

GENESIS™ 3100, 3100X SEMI-CUSTOM IC

The Genesis 3100 and 3100X are linear semi-custom arrays designed specifically for micropower applications. Using Ion-Implant technology, the chip provides more than 5 megohms of resistance. A unique metal interconnect mask is used to define the finished custom IC. The 3100X is an extended performance version that doubles the useful operating current range of the NPN transistors.

- TOTAL COMPONENTS: 479
- CHIP SIZE (mils): 79 x 107
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 22
- NPN TRANSISTORS: 85
- PNP TRANSISTORS: 36
- POWER NPN TRANSISTORS: 3
- TOTAL RESISTORS: 355
  - 86 Diffused
  - 261 Ion-Implant
  - 8 Pinch



9

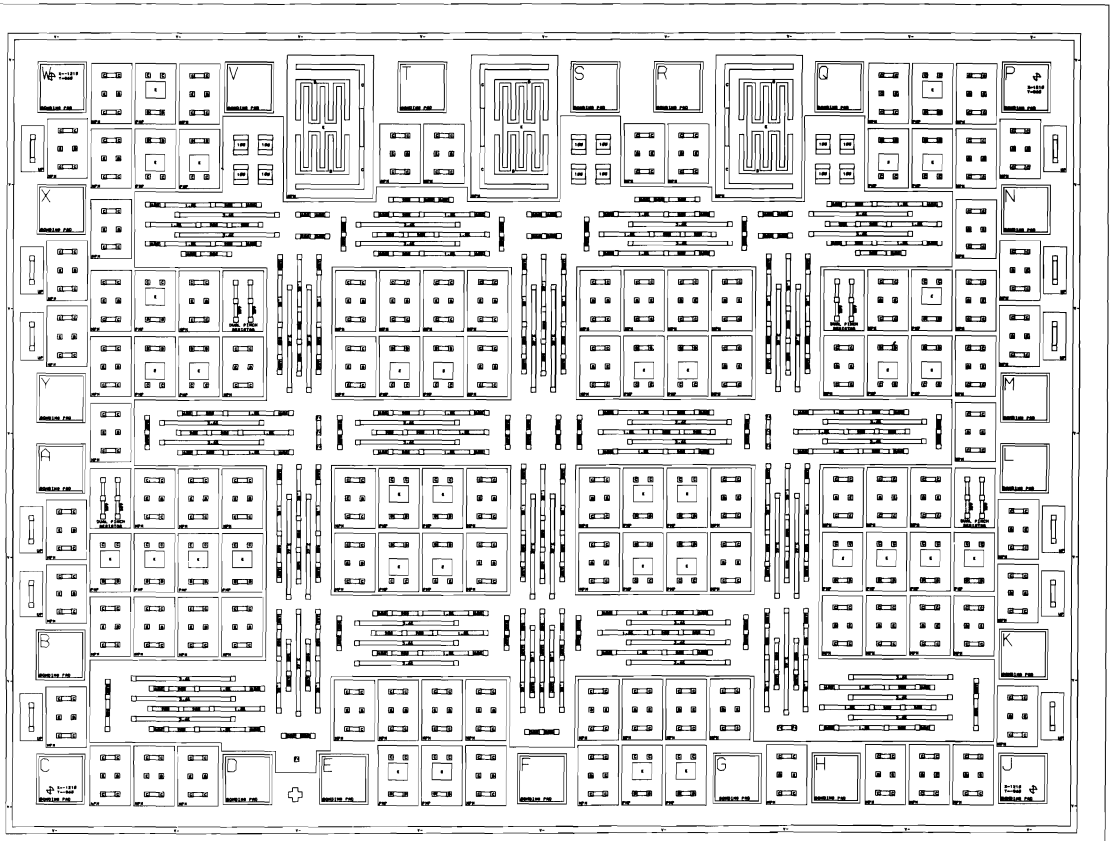
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY

GENESIS™ 3200L, 3200LX SEMI-CUSTOM IC

The Genesis 3200L and 3200LX are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. A unique metal interconnect mask is used to define the finished custom IC. The 3200LX is an extended performance version that doubles the useful operating current range of the NPN transistors.

- TOTAL COMPONENTS: 479
- CHIP SIZE (mils): 79 x 107
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 22
- NPN TRANSISTORS: 85
- PNP TRANSISTORS: 36
- POWER NPN TRANSISTORS: 3
- TOTAL RESISTORS: 355



CSC™ CHERRY SEMICONDUCTOR

LINEAR
HIGH SPEED
BIPOLAR ARRAY

GENESIS™ 3300 SEMICUSTOM IC

Designed for the integration of higher performance linear functions, the GENESIS™ LS One GHz process provides a component density 25% greater than conventional linear arrays. Yet they retain the flexible transistor geometries that allow most integrations to be accomplished with a low cost single dedicated interconnect mask approach. For dense applications, two layer metal (three dedicated mask levels) is available. The arrays feature four transistor geometries arranged in a macrocell matrix, combined with a wide range of diffused and ion implant resistor values.

- 1 GHz process (NPN F_T)
- Single/two layer metal options permit cost/density tradeoff
- Base diffused and ion implant resistors permit practical values from 50Ω to 200KΩ, on the same chip
- Die size optimized for narrow (.150" wide) SOIC package
- Macrocell architecture
- Deep collector wall diffusion reduces saturation and crossunder resistance
- Power supply range 1 to 14V

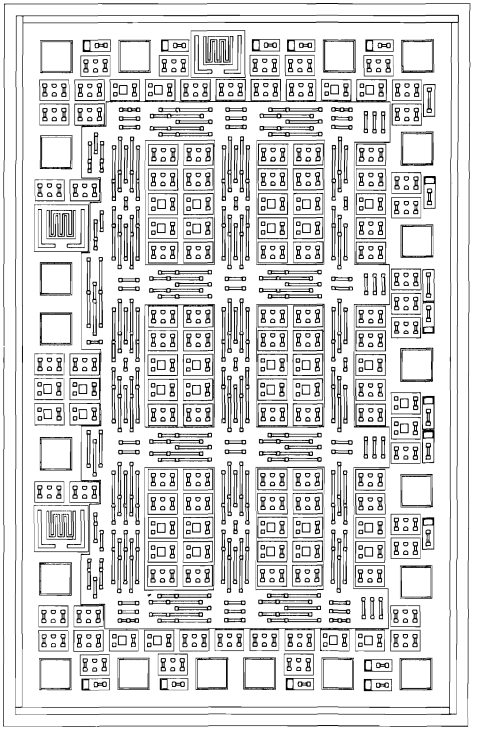
Component List

Transistors	
Small NPN	89
Medium (100mA) NPN	3
Lateral PNP, 2 collector	42
Substrate PNP	15
Resistors	
450Ω, diffused	13
900Ω, diffused	130
1,8KΩ, diffused	100
10KΩ, implant	15
20KΩ, implant	26

Key Performance Characteristics

Process		bipolar, shallow base
N+ sinker[1] diffusion		standard
Max power supply voltage		14V
Metal interconnect levels		1 or 2[2]
Metal pitch, μM		14
Metal resistance, mΩ/square		40,60[3]
Small NPN transistor		
V_{CEO}, min		12
Recommended operating current range	Min, nA	10
	Max, mA	3
Minimum H_{FE} at I_E = 100μA		50
F_T, @ 1mA, 5V (MHz)		1000
V_{BE} match, adjacent transistors (mV)		5
Lateral PNP transistor		
V_{CEO}, min		14
Recommended operating current range	Min, nA	50
	Max, μA	250
Minimum H_{FE} at I_E = 40μA		12
F_T, @ 1mA, 5V (MHz)		5
V_{BE} match, adjacent transistors (mV)		5

Notes:
1. Also designated as "well", "plug", "deep N+"
2. Two layer metal is optional
3. Second value applies to the first (lower) interconnect level of a two-level metal design



Die size: 114 x 74 mils

20 bonding pads

9

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

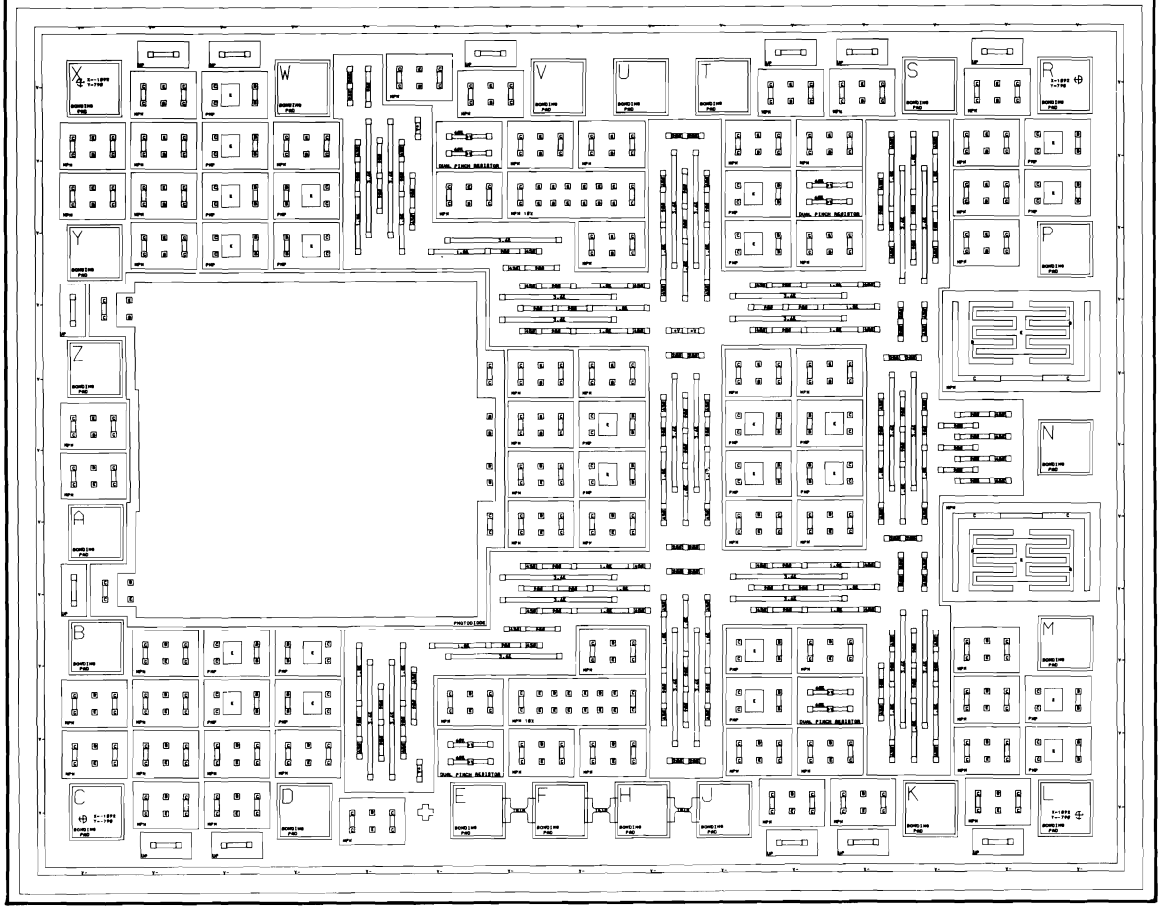
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY
OPTOELECTRONIC

GENESIS™ 3500, 3500X SEMI-CUSTOM IC

The Genesis 3500 and 3500X are opto-electronic circuits incorporating a photo-detector and an uncommitted array of transistors and resistors on a single monolithic chip. They are suited for a variety of applications requiring a light sensitive function combined with additional signal processing capability. The 3500X is an extended performance version that doubles the useful current range of the NPN transistors.

- TOTAL COMPONENTS: 299
- CHIP SIZE (mils): 75 x 97
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 22
- NPN TRANSISTORS: 59
- PNP TRANSISTORS: 24
- POWER NPN TRANSISTORS: 2
- TOTAL RESISTORS: 214
- ON-CHIP PHOTODETECTOR: 1



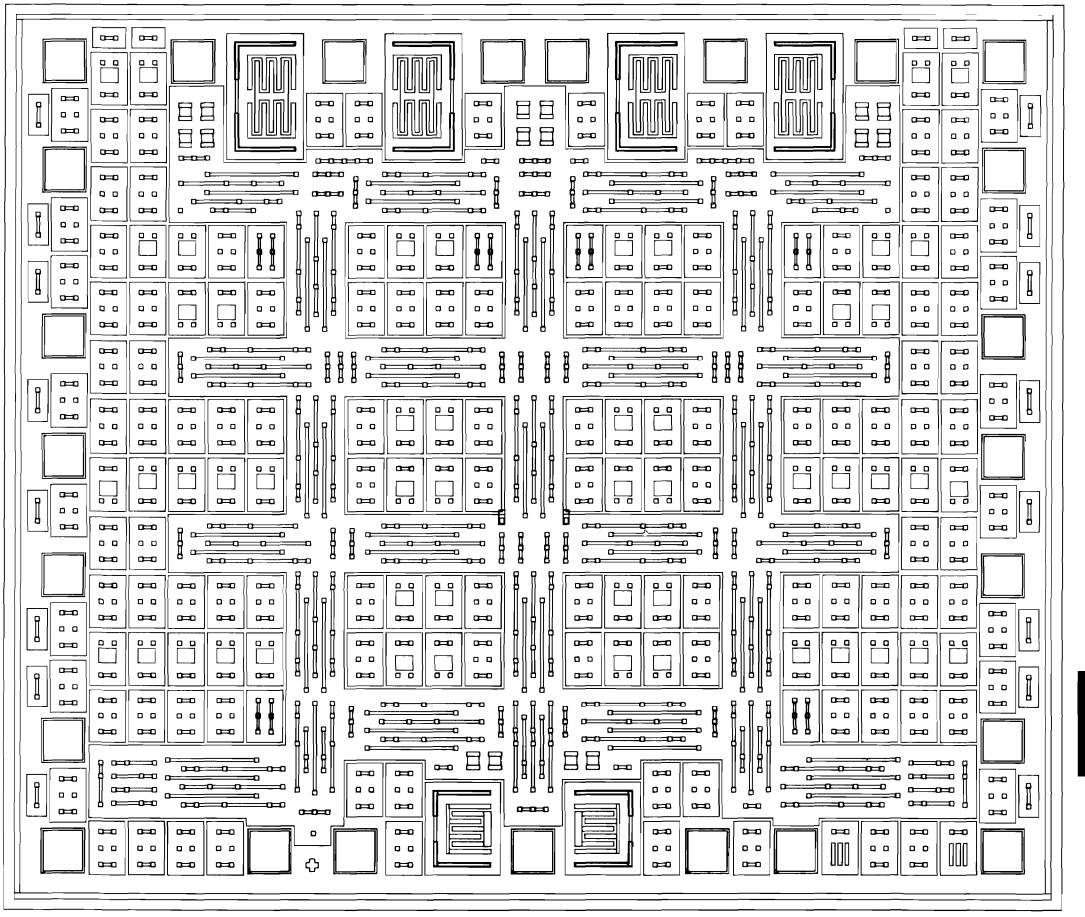
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY

GENESIS™ 3600, 3600X SEMI-CUSTOM IC

The Genesis 3600 and 3600X are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. A unique metal interconnect mask is used to define the finished custom IC. The 3600X is an extended performance version that doubles the useful operating current range of the NPN transistors. Of special interest is the inclusion of two low-noise NPN transistors.

- TOTAL COMPONENTS: 669
- CHIP SIZE (mils): 98 x 115
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 25
- NPN TRANSISTORS: 117
- PNP TRANSISTORS: 52
- POWER NPN TRANSISTORS: 6
- TOTAL RESISTORS: 494



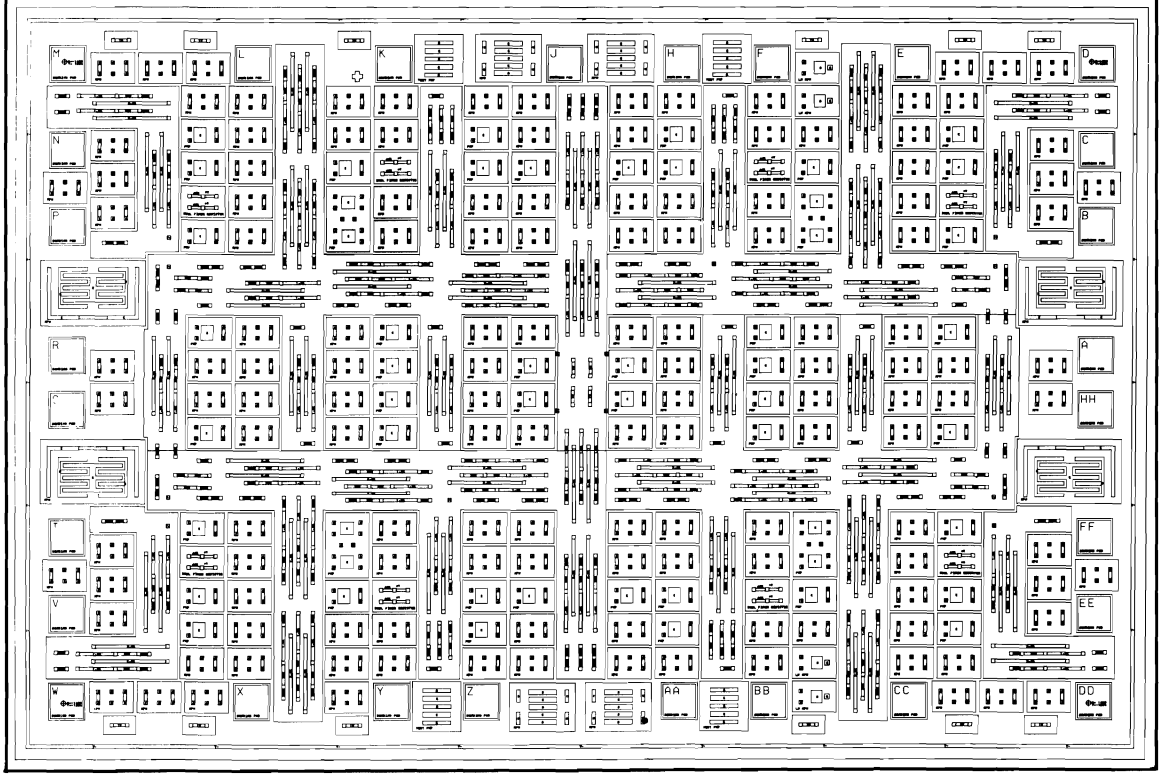
CHERRY SEMICONDUCTOR

LINEAR
BIPOLAR ARRAY

GENESIS™ 4000M, 4000MX SEMI-CUSTOM IC

The Genesis 4000M and 4000MX are uncommitted arrays of transistors and resistors fabricated on a single monolithic chip. A unique metal interconnect mask is used to define the finished custom IC. The 4000MX is an extended performance version that doubles the useful operating current range of the NPN transistors.

- TOTAL COMPONENTS: 801
- CHIP SIZE (mils): 96 x 147
- MAX OPERATING VOLTAGE: 20V
- BONDING PADS: 28
- NPN TRANSISTORS: 141
- LOW NOISE NPN TRANSISTORS: 4
- PNP TRANSISTORS: 52
- SUBSTRATE PNP TRANSISTORS: 4
- POWER NPN TRANSISTORS: 8
- TOTAL RESISTORS: 592



CSC™ CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY

GENESIS™ 5000 SEMI-CUSTOM IC

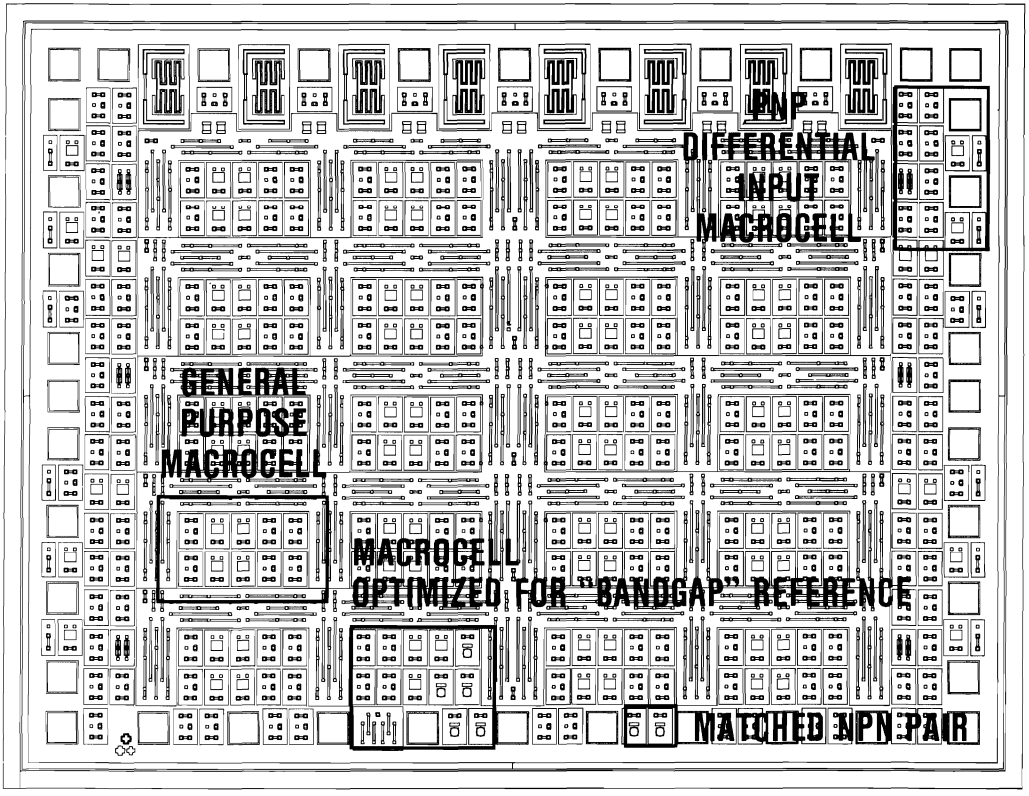
Intended for the integration of complex circuits, the GENESIS™ 5000 linear array has over 300 transistors and includes 20 macrocell "tiles" organized in a 4 x 5 matrix. This approach allows circuit functions to be replicated simply by transferring the layout to another cell. Nineteen of the macrocells are identical, while one is optimized for configuration as a "bandgap" voltage reference.

Eight power transistors, located along one edge of the die, permit an octal buffer, dual "H" bridge driver, or quad push-pull output stage to be realized, at output currents up to 200mA.

Additional features include low-offset matched NPN pairs and substrate PNP pairs for use in the input stages of op amps and comparators.

- TOTAL ACTIVE COMPONENTS: 314
- TOTAL COMPONENTS: 1178
- CHIP SIZE (mils): 163 x 122
- POWER SUPPLY RANGE: 1.0 to 20V
- BONDING PADS: 40
- SMALL NPN TRANSISTORS: 199
- POWER NPN TRANSISTORS: 8
- LATERAL PNP TRANSISTORS: 95 (dual collector)
- SUBSTRATE PNP TRANSISTORS: 12
- TOTAL RESISTANCE (exclusive of pinch resistors): 1107KΩ

132	3.6KΩ
152	1.8KΩ
268	900Ω
228	450Ω
64	240Ω
14	100Ω
6	dual 60K pinch



Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
(401) 885-3600 Telefax (401) 885-5786 Telex WUI 6817157

CSC™ CHERRY SEMICONDUCTOR

LINEAR
HIGH SPEED
BIPOLAR ARRAY

GENESIS™ 5200 SEMICUSTOM IC

Designed for the integration of higher performance linear functions, the GENESIS™ LS One GHz process provides a component density 25% greater than conventional linear arrays. Yet they retain the flexible transistor geometries that allow most integrations to be accomplished with a low cost single dedicated interconnect mask approach. For dense applications, two layer metal (three dedicated mask levels) is available. The arrays feature four transistor geometries arranged in a macrocell matrix, combined with a wide range of diffused and ion implant resistor values. GENESIS™ 5200 contains more than 25 general purpose cells, as well as specialized voltage reference and fuse link (for active trim at wafer probe) sections.

- 1 GHz process (NPN F_T)
- Single/two layer metal options permit cost/density tradeoff
- Base diffused and ion implant resistors permit practical values from 50Ω to 2MΩ, on the same chip
- Macrocell architecture
- Optimized voltage reference and comparator macrocells
- Deep collector wall diffusion reduces saturation and crossunder resistance
- Power supply range 1 to 14V

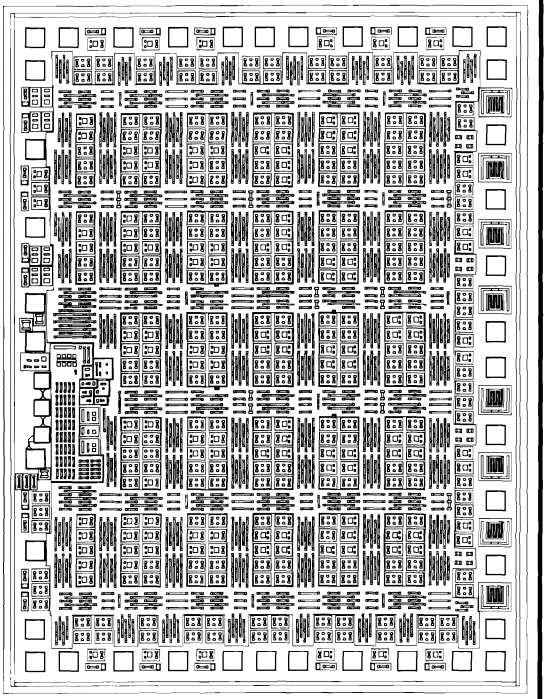
Component List

Transistors	
Small NPN	226
Medium (100mA) NPN	8
Lateral PNP, 2 collector	130
Substrate PNP	22
Resistors	
200Ω, diffused	16
240Ω, diffused	16
900Ω, diffused	910
10KΩ, implant	8
20KΩ, implant	4
22KΩ, implant	6
30KΩ, implant	4
24KΩ, implant	66

Key Performance Characteristics

Process		bipolar, shallow base
N+ sinker[1] diffusion		standard
Max power supply voltage		14V
Metal interconnect levels		1 or 2[2]
Metal pitch, μM		14
Metal resistance, mΩ/square		40,60[3]
Small NPN transistor		
V_{CEO}, min		12
Recommended operating current range	Min, nA	10
	Max, mA	3
Minimum H_{FE} at I_E = 100μA		50
F_T, @ 1mA, 5V (MHz)		1000
V_{BE} match, adjacent transistors (mV)		5
Lateral PNP transistor		
V_{CEO}, min		14
Recommended operating current range	Min, nA	50
	Max, μA	250
Minimum H_{FE} at I_E = 40μA		12
F_T, @ 1mA, 5V (MHz)		5
V_{BE} match, adjacent transistors (mV)		5

Notes:
1. Also designated as "well", "plug", "deep N+"
2. Two layer metal is optional
3. Second value applies to the first (lower) interconnect level of a two-level metal design



Die size: 181 x 140 mils

40 bonding pads

Cherry Semiconductor Corporation, 2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax (401)885-5786 Telex WUI 6817157

CSC™ CHERRY SEMICONDUCTOR

GENESIS™ 6000 Series

5 AMP SMART POWER MULTICHIP ARRAY

FEATURES

- Power, linear and logic capability in the same package
- 5A max power output capability
- Overcurrent and overvoltage protection available
- Thermal shutdown function available

APPLICATIONS

- DC and stepper motor controllers
- Lamp drivers/timers
- Relay, solenoid, triac drivers/controllers
- DC to DC converter control circuits
- Smart power amplifier
- Smart voltage regulator

DESCRIPTION

The GENESIS™ 6000 smart power multichip array merges high current, analog, and I^2L logic functions in a 15 lead MULTIWATT® or a 20 or 24 lead Batwing SO power package (Figure 1A). The multichip array package contains 2 power NPN transistors, capable of sinking 2.5A each or 5A total and any one of more than 12 GENESIS arrays

By choosing a linear/digital bipolar array, the designer can realize smart power circuitry containing 98 I^2L logic gates and 198 linear transistors. By choosing a pure linear bipolar array, the designer can realize signal processing and power circuitry requiring up to 314 small and medium current NPN and PNP transistors (see Table 1).

With the flexibility this multichip array provides, the designer can quickly implement customized circuits which control and drive high current, high voltage resistive and reactive loads e.g. DC and stepper motors, relays, solenoids, triacs, and incandescent lamps. Overcurrent, over- and undervoltage protection, and thermal shutdown can also be included on chip.

POWER TRANSISTOR CHARACTERISTICS

Absolute Maximum Ratings

BV_{CEO}	50V
DC Collector Current	2.5A
Junction Temperature	150°C
Operating Temperature	-55 to +125°C
Storage Temperature	-55 to +150°C

MULTICHIP ARRAY IN A 24 LEAD BATWING SO

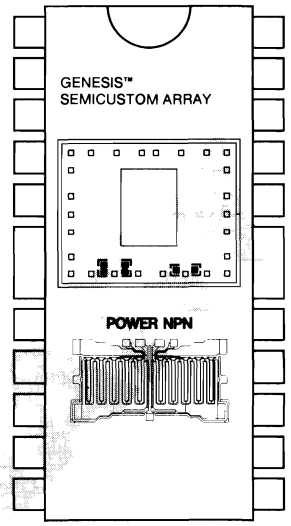


Figure 1A

TYPICAL POWER TRANSISTOR CURVES T_a=25°C

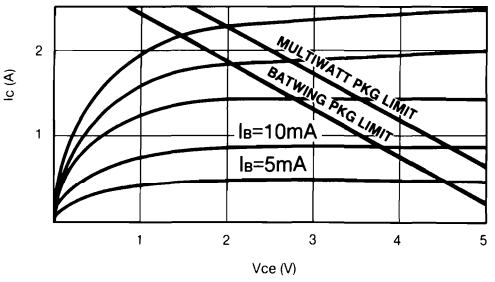


Figure 1B

9

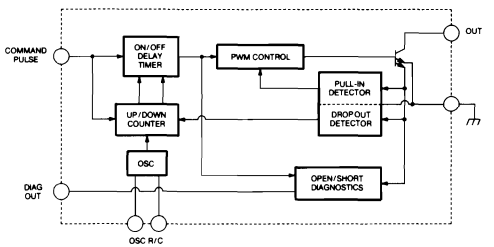
MULTICHIP COMPATIBLE GENESIS™ SEMICUSTOM ARRAYS

TYPE NUMBER	ARRAY TYPE	DIE SIZE (Mils)	Vcc RANGE (V)	BOND PADS	I^2L GATES	I/O PORTS	DIODES	TRANSISTORS			RESISTORS		
								NPN	PNP	PWR NPN	DIFFUSED	ION IMPLANT	PINCH
1100	DIGITAL & LINEAR	98 x 124	1-12	26	64	—	—	98	41	4	339	—	8
1500	DIGITAL & LINEAR	123 x 140	1-12	30	98	—	—	122	72	4	462	—	2
2500G	LINEAR	75 x 79	1-20	18	—	—	—	58	18	2	239	—	8
3000F	LINEAR	91 x 110	1-20	24	—	—	—	92	36	4	296	—	9
3100	(MICROPOWER) LINEAR	79 x 107	1-20	22	—	—	—	85	36	3	86	261	8
3200L	LINEAR	79 x 107	1-20	22	—	—	—	85	36	3	347	—	8
3500	(OPTO) LINEAR ARRAY	75 x 97	1-20	22	—	—	—	59	24	2	206	—	8
3600	LINEAR	98 x 115	1-20	25	—	—	—	117	52	6	482	—	12
4000M	LINEAR	96 x 147	1-20	28	—	—	—	145	56	8	576	—	16
5000	LINEAR	122 x 163	1-20	40	—	—	—	199	107	8	858	—	6
7600	(L/LS) LINEAR	98 x 118	1-15	25	—	—	10 DUAL	138	26	4	384	139	—
8000	(H.V.) LINEAR	105 x 123	1-50	23	—	—	2 ZENER 28V	60	32	2	427	—	—

Table 1

SPECIFIC APPLICATION EXAMPLES

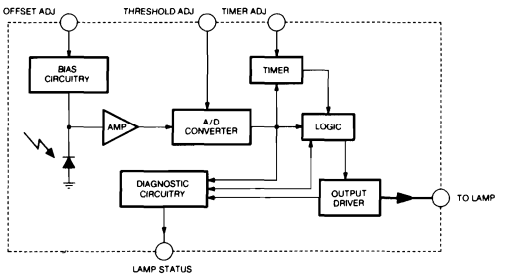
The Smart Solenoid Driver



Circuit Features

- Solenoid Driver corrects for solenoid delays
- PWM Control permits output driver to sink 5A
- Diagnostic capabilities
- Microprocessor Compatible
- Continuous Control due to Feedback in Circuit

The Smart Lamp Driver with On Chip Sensor



Circuit Features

- Protection circuitry limits the output driver and prevents thermal runaway
- On board sensor
- Microprocessor compatible diagnostics signal

CSC™ CHERRY SEMICONDUCTOR

2000 South County Trail, East Greenwich, Rhode Island 02818
Tel: (401)885-3600 Telefax(401)885-5786 Telex WUI 6817157

Our Sales Representative in Your Area is:

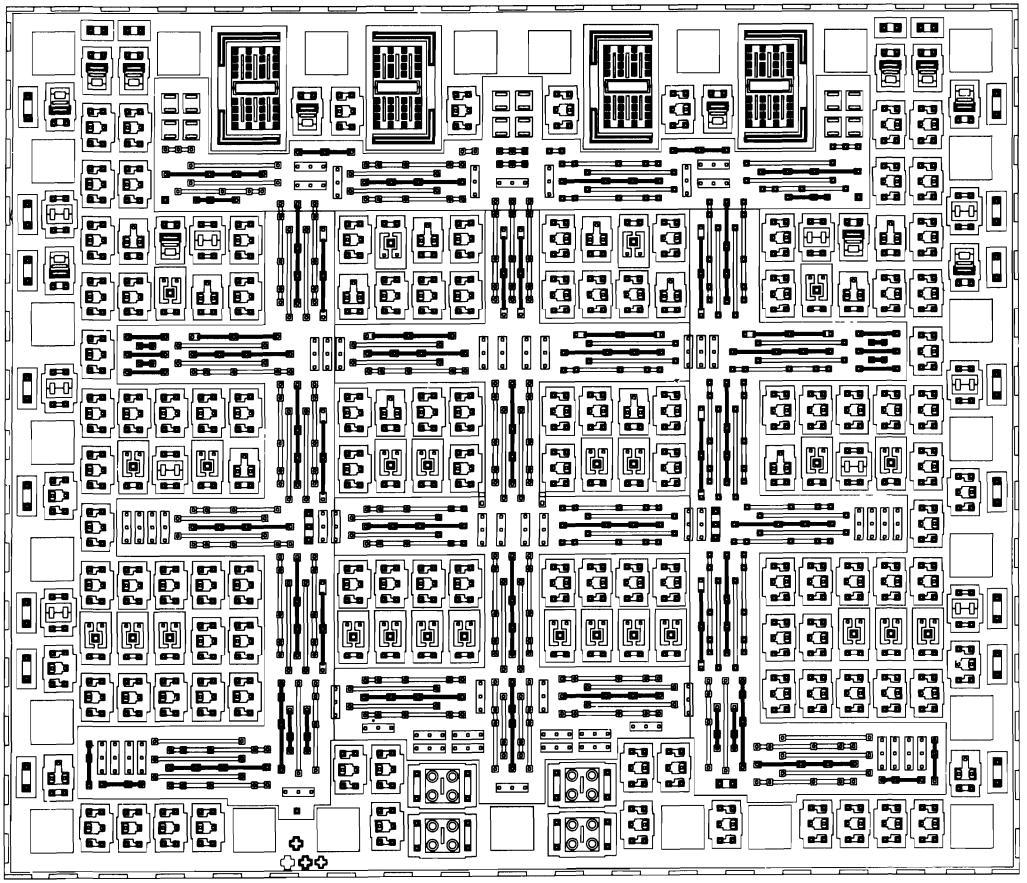
CHERRY SEMICONDUCTOR

LINEAR BIPOLAR ARRAY (L/LS)

GENESIS™ 7600 SEMI-CUSTOM IC

The 7600 L/LS combines a high frequency linear process with LSTTL gate equivalent capabilities. The gain-bandwidth product of the small NPN transistors is typically 800 MHz. The resistor complement includes 384 diffused resistors with a combined value of 525K, and 139 ion-implant resistors with a combined value of over 2 megohms. The variety and characteristics of the 701 total components make the 7600 an especially versatile, and high performance chip for a wide range of linear applications.

- TOTAL COMPONENTS: 701
- CHIP SIZE (mils): 98 x 118
- MAX OPERATING VOLTAGE: 15V
- BONDING PADS: 25
- NPN TRANSISTORS: 138
- PNP TRANSISTORS: 26
- POWER NPN TRANSISTORS: 4
- DUAL DIODES: 10
- TOTAL RESISTORS: 523



CHERRY SEMICONDUCTOR

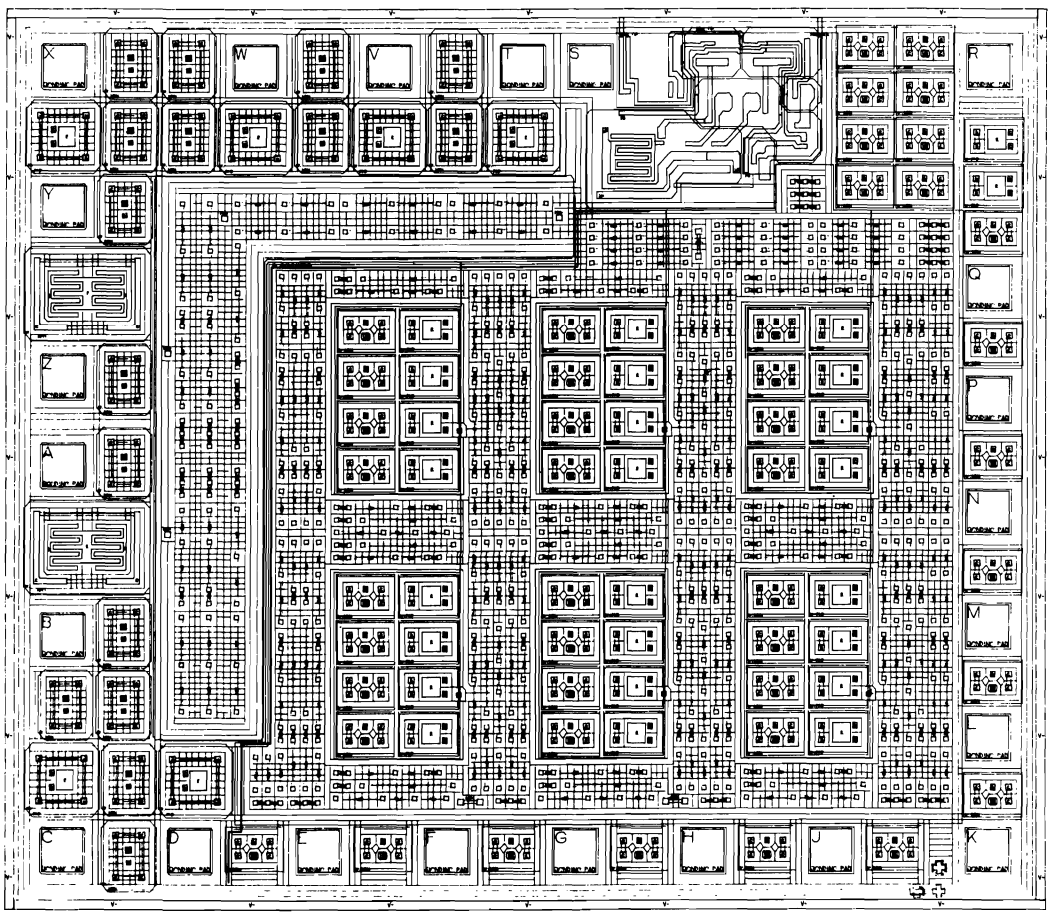
LINEAR BIPOLAR ARRAY (50V)

GENESIS™ 8000 SEMICUSTOM IC

The GENESIS 8000 is a linear semicustom array designed specifically for higher voltage applications, such as industrial control and automotive electronics. The chip can operate at power supply voltages up to 50 volts. A programmable bandgap reference/regulator, with a 20mA output current capability, is included on the array. Programmable range is 1.2 to 20V.

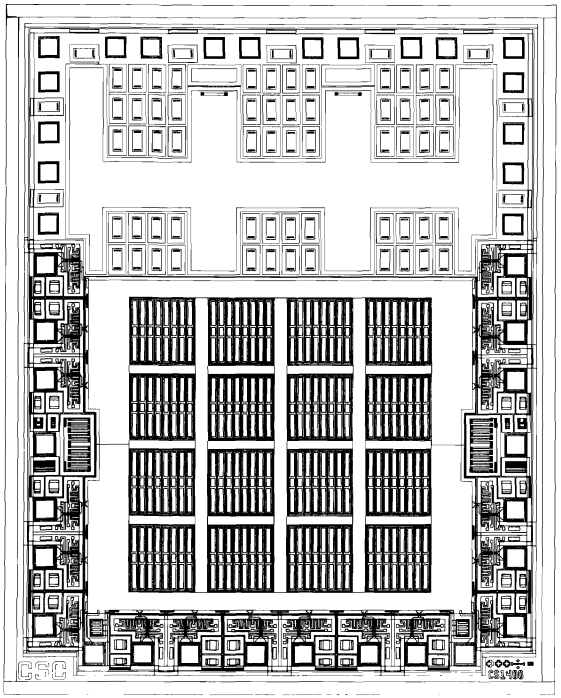
To improve utilization density relative to conventional high voltage linear arrays, the chip is designed in two separate sections with different voltage capabilities. The 50V section contains the voltage regulator plus 24 uncommitted transistors (16 NPN, 6 PNP and 2 power NPN). The remainder of the array has a 20V operating voltage limit. Typically, the high voltage devices are used to realize input/output interfaces, buffers, and load drivers, while the functional performance circuits are accomplished with the more densely packed 20V components.

- TOTAL COMPONENTS: 522
- CHIP SIZE (mils): 105 x 123
- MAX OPERATING VOLTAGE: 50V
- BONDING PADS: 23
- NPN TRANSISTORS: 60
- PNP TRANSISTORS: 32
- POWER NPN TRANSISTORS: 2
- RESISTORS: 427 (508K TOTAL)
- BANDGAP REFERENCE: 1.25V TO 20V, UP TO 20 mA



MICROPOWER I²L DIGITAL/LINEAR ARRAY

ROBERT J. MAIGRET
Manager, Semicustom Programs



GENESIS™ 1400

A MICROPOWER LINEAR/DIGITAL SEMICUSTOM ARRAY

The CS-1400 is a bipolar semicustom chip that combines a 256 gate logic array, a 69 transistor linear array, and 18 programmable interface cells on a single IC. Whereas the typical gate array is "personalized" with a single discretionary inter-connect mask, the CS-1400 is *multi-mask* programmable. This approach offers several significant advantages:

- Enhanced packing density of the integrated injection logic array, with gate utilization levels of 90% readily attainable.
- Selectable transistor designations and multiple device geometries - only the location and overall size of the linear array transistors are predetermined.
- Open resistor field - the value, mix, location, width, and orientation of the linear array resistors are discretionary rather than fixed.

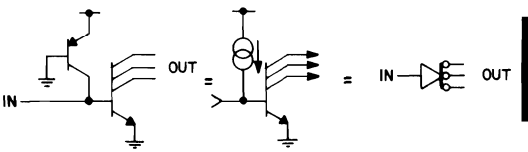
A key advantage of integrated injection logic is programmable power consumption/gate delay. The CS-1400 gates can be operated at currents in the range of 10nA to 400uA (per gate). Corresponding propogation delays are approximately 100uS to 40nS. For low frequency applications, the power consumption characteristics are comparable to CMOS arrays (the operating voltage of the bipolar I²L gates is only approximately 650 millivolts). The successful integration of a low-power linear/digital system is often dependent on the achievement of similar power supply current reduction in the linear section. The design of linear functions for minimum current drain is extremely difficult, given the range of diffused resistor values typically available on semicustom chips. Sheet resistivity is typically 125 to 200 ohms/square, and the largest practical value for a diffused (base) resistor is 50K to 100K. Larger values are possible with pinch resistors, but their poor tolerance is inappropriate in many cases.

The CSL-1400 is a *micropower* version of the CS-1400 that addresses the challenge of low power linear circuit implementation by providing *ion-implanted* as well as diffused resistors. The ion implant resistors have a standard sheet resistivity of 2K ohms/square; values up to 0.5 megohm are practical. An alternate sheet resistivity of 5K ohms/square is available on special order. Both implant and base resistors can be intermixed in a circuit; there is no difference in layout rules.

CSL 1400 MASK LEVELS

GENERIC	DISCRETIONARY
BURIED N	BASE
ISOLATION	ION IMPLANT
DEEP N(WELL)	EMITTER
PASSIVATION	CONTACT
	METAL INTERCONNECT

I²L GATE

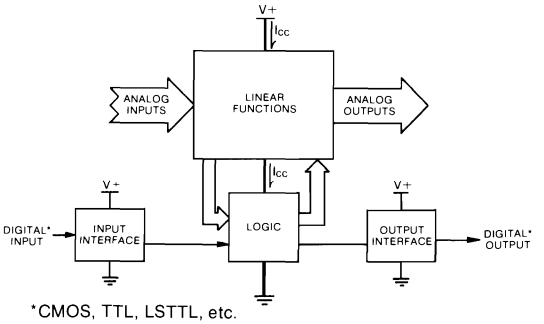


9

ACHIEVING MINIMUM SUPPLY CURRENT WITH THE CSL-1400

Integrated injection logic exhibits some unique characteristics that provide important advantages to the micropower linear/digital circuit designer. The most significant of these is the concept of *stacked circuit functions*. This is simply a design technique whereby the logic and linear functions are in *series*, rather than in parallel across the power supply rails. The feasibility of stacking results from the low voltage drop of the digital gates, approximately 650 millivolts. This drop is essentially independent of the number of gates.

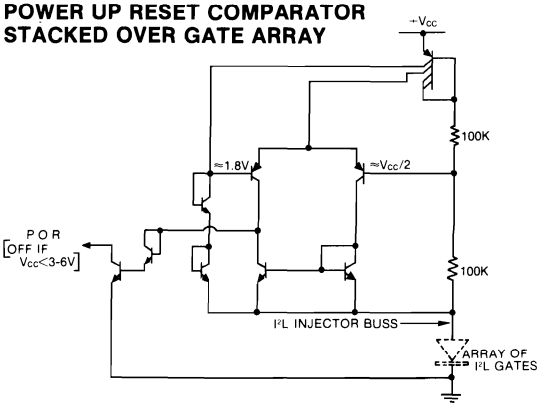
CONCEPT OF FUNCTION "STACKING"



*CMOS, TTL, LSTTL, etc.

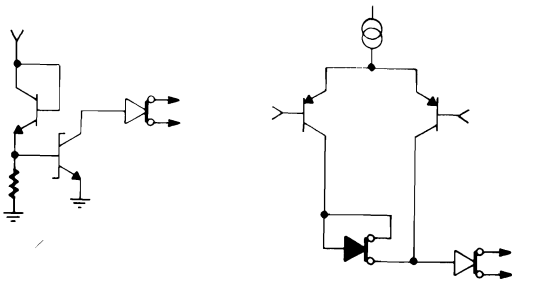
Utilizing *stacked functions*, the entire digital content of a complex IC can be inserted in the negative buss return of one of the analog blocks. Thus, all of the logic can be accomplished *without any contribution to the total IC current drain*, since we are re-using current already committed to an analog function.

POWER UP RESET COMPARATOR STACKED OVER GATE ARRAY

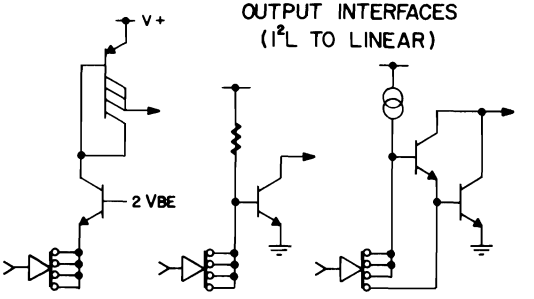


In the case of the analog circuitry, supply current management techniques include liberal use of ion implant resistors, combined with active loads. With an active current sink consisting of a diode biased NPN transistor and implant emitter resistor, programmed current levels as low as 10nA are practical. I²L gates can also be employed as constant current sinks, a technique that eliminates the emitter resistor altogether.

INPUT INTERFACES (LINEAR TO I²L)



OUTPUT INTERFACES (I²L TO LINEAR)



CSL-1400 integrations can usually be designed to require lower worst-case power supply current than an equivalent discrete realization of the circuit comprised of standard low power linear and digital CMOS devices. While the typical standby current of 400 series CMOS gates is very low, guaranteed worst-case consumption is 5-10uA per package at +20°C and 25-75uA at +85°C. By contrast, the equivalent logic functions integrated as a stacked CSL-1400 digital block consume effectively zero standby current at both temperatures. The analog circuitry can generally be designed to exhibit standby current identical to a discrete equivalent. In many systems, further current reductions can be accomplished by power-up and power-down techniques that selectively deactivate circuits in the standby mode.

APPLICATIONS

This chip is most suitable for systems that will tolerate digital gate propogation delays on the order of a microsecond for most of the logic. The higher injector currents required to improve the response time predicate standby current levels that are inconsistent with a micropower circuit. In cases where fast performance is limited to a percentage of the total gate count, separate injector rails can be employed, thereby minimizing the overall current drain impact.

The advantages of micropower linear/I²L are best realized in applications where system operating power is derived from limited capacity sources, such as batteries, stored capacitor charge, and data line scavenging (where a single conductor is used for data in, data out, and power). Typical of these applications are security subsystems, transducer interfaces, and low frequency infrared data transmitters.

3500 OPTOELECTRONIC ARRAY

GENESIS™

ROBERT J. MAIGRET

Manager, Semi-custom Programs

INTRODUCTION

Semi-custom Arrays, by offering the advantages of a proprietary circuit at a fraction of the tooling cost and time of a "full custom" program, have extended the availability and practicality of Custom ICs to a broad spectrum of new applications. Present arrays are, for the most part, "general purpose" in nature, designed for universal applicability. This is especially true in the case of linear arrays; whereas some degree of specialization is provided in the digital realm by various technology options (ECL, CMOS, I^2L, etc.).

The GENESIS 3500, by contrast, is a linear special purpose semi-custom array, designed expressly for optoeletronic applications. Fabricated with bipolar technology, it features an integral "on chip" silicon photodetector

Applications encompass both linear systems and pulsed light to signal converters operating at frequencies up to 100 KH_z. Device "personalization" is accomplished with a unique metal interconnect pattern; wafers are prefabricated up to this processing step and held in inventory.

DESCRIPTION

The GENESIS 3500 is an uncommitted linear array consisting of transistors and resistors combined with a photodetector on a single monolithic chip. Figure 1 is an overall drawing of the array; Figure 2 provides a listing of components. Die size is 75 x 97 mils; the photodetector is approximately 29 x 29 mils, with an active area of $0.5mm^2$. Two high current NPN transistors provide the capability to drive relays and lamps directly.

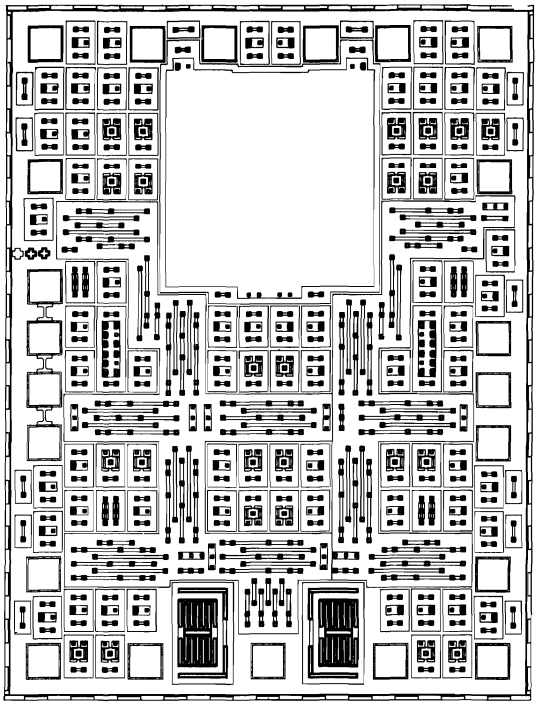


FIGURE 1

22	Bonding pads	20	200 ohm
57	Small NPN transistors	60	450 ohm
24	PNP Transistors	64	900 ohm
2	NPN Transistors, 10X	36	1.8K
2	High current NPN transistors	26	3.6K
224	Resistors	8	60K pinch

FIGURE 2

EXTENDED PERFORMANCE (3500x)

The 3500 is available in two versions, Standard and Extended Performance. The standard version is fabricated with a 7 mask Bipolar process, a process essentially identical to that used to manufacture linear semi-custom arrays available from several suppliers. The extended performance option differs from the traditional process by addition of a collector wall (or "sinker") masking and deep N+ diffusion. The primary beneficiary of this added step is the NPN transistors. The collector wall diffusion provides a low resistance path for collector current to reach interconnect metal deposited on the top surface of the chip. The net effect is an increase of up to 100% in the operating current range of the NPN devices, combined with up to a 50% reduction in their collector emitter saturation voltage. This translates to enhanced load current drive capability without an increase in chip power dissipation. Figure 3 depicts a cross sectional view of NPN transistors fabricated with the standard and extended performance processes.An ancillary benefit derived from the collector wall diffusion is a thicker insulating oxide growth over the collector underpasses. This increases the typical crossunder sustaining voltage from 200 to over 500 volts, thereby enhancing the ability of the IC to withstand supply and input voltage transients without damage.

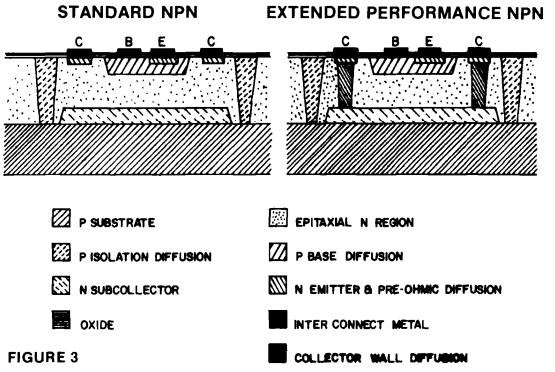


FIGURE 3

9

COMPONENT CHARACTERISTICS

Figure 4 summarizes the electrical performance parameters of the components comprising the standard and extended performance versions of the array The values given for NPN saturation voltage assume that all collector contacts are used. The lateral PNP transistors, which have 2 independent collectors are characterized with the collectors connected together

COMPONENT ELECTRICAL CHARACTERISTICS

TRANSISTORS	SS NPN		LATERAL PNP		POWER NPN	
	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS	TYP	3 SIGMA LIMITS
V_{CE} V	25	20	35	20	25	20
I_{CEO} @ 15V A	001	05	005	0 1	02	1 0
V_{EBO} V	7 0	6 5-7 5	35	–	7 0	6 5-7 5
h_{FE} @ 10 µA 5V	100	40-300	25	7-80	–	–
h_{FE} @ 100µA 5V	120	60-360	20	5-80	–	–
h_{FE} @ 10mA 5V	100	40-300	–	–	100	40-200
h_{FE} @ 100mA 5V	–	–	–	–	100	40-200
R_{SAT} @ 10mA Ω	50	30-80	500 (@ 0 1mA)		6	4-10
R_{SAT} @ 10mA # Ω	25	20-60	–	–	4	2-6
R_{SAT} @ 100mA Ω	–	–	–	–	6	4-10
R_{SAT} @ 100mA # Ω	–	–	–	–	4	2-6
f_T MHz	400	–	4	–	350	–
OPERATING CURRENT RANGE	0 1µA to 20mA		0 1µA to 1mA		1µA to 150mA	
OPERATING CURRENT RANGE #	0 1µA to 50mA		0 1µA to 1mA		1µA to 300mA	

Extended performance version

RESISTORS	1.8K		3.6K		30K, 60K	
	TYP	3 SIGMA	TYP	3 SIGMA	TYP	3 SIGMA
ABSOLUTE TOLERANCE	10%	·25%	·10%	·25%	·50%	+100% −50%
MATCHING* IDENTICAL VALUE	·0.8%	·3%	·0.8%	·3%	·20%	–
TEMP %/°C COEFFICIENT	+0 14	+ 08- 2	+0 14	+ 08- 2	+1 0	–
BREAKDOWN VOLTAGE—VOLTS	35	–	35	–	6.5	6-8
MAX D.C VOLTAGE DROP—VOLTS	–	13.4	–	19	–	6.0
	100Ω, 200Ω		450Ω		900Ω	
	TYP	3 SIGMA	TYP	3 SIGMA	TYP	3 SIGMA
ABSOLUTE TOLERANCE	15%	·30%	10%	·25%	10%	·25%
MATCHING* IDENTICAL VALUE	·1 5%	·5%	·1%	·3%	·0.8%	·3%
TEMP %/°C COEFFICIENT	+0 14	+.08- 2	+0 14	+ 08- 2	+0.14	+.08- 2
BREAKDOWN VOLTAGE—VOLTS	35	–	35	–	35	–
MAX D C VOLTAGE DROP—VOLTS	–	4.5	–	6.7	–	9.5

*WITH IDENTICAL ORIENTATION

FIGURE 4

PHOTODETECTOR

The GENESIS 3500 photodetector is designed to permit connection as a photodiode or phototransistor The diode configuration exhibits superior linearity and temperature stability, but lower sensitivity than the phototransistor connection. The detector consists of an NPN transistor with a large area base-collector junction (see Fig. 5 for equivalent circuit) The photodiode configuration is obtained by leaving the emitter contact open.

Note that in addition to the base-collector photosensitive junction, there is a parasitic photodiode (collector-substrate). If the detector is configured as a photodiode with the collector current being monitored, the collector-base and collector-substrate photosensors are in parallel. This increases the sensitivity slightly (5-10%), but approximately doubles the capacitance. Configurations that place the collector-substrate junction between two unmeasured nodes are preferred when response speed must be optimized.

PHOTODETECTOR EQUIVALENT CIRCUIT

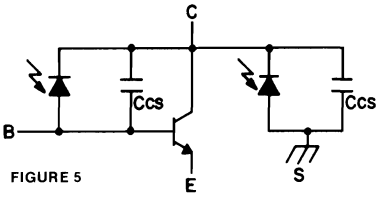


FIGURE 5

PHOTODETECTOR CHARACTERISTICS

Usable Spectrum	450-1050	nM
Radiometric Sensitivity at 900nM	2 (200*)	nA/mW/cM²
Photopic Sensitivity	0.35 (350*)	nA/LUX
Dark Current @ 0 6V	0 1 (10*)	nA
Capacitance, C_{C-B} @ 0V	55	pF
Capacitance, C_{C-S} @ 0V	60	pF

*(Phototransistor Configuration)

FIGURE 6

SPECIAL COMPONENTS

The 3500 contains two NPN transistors with 10X emitters. These are particularly useful for current scaling circuits and bandgap voltage regulators. Since there are 10 separate identical emitter sections, they can be used selectively to obtain emitter ratios from 2:1 to 10:1. Each emitter section is identical in size to the emitter of the small NPN transistors.

Figure 7B is a drawing of the fuse link array available on each chip. These links can be selectively opened during the wafer probe test operation. This provides the ability to active trim a circuit electrical or optical parameter.

This feature is ideal for applications such as adjusting an on-chip voltage reference, trimming the trip point of a light-sensitive comparator function, or reducing the offset voltage of an operational amplifier

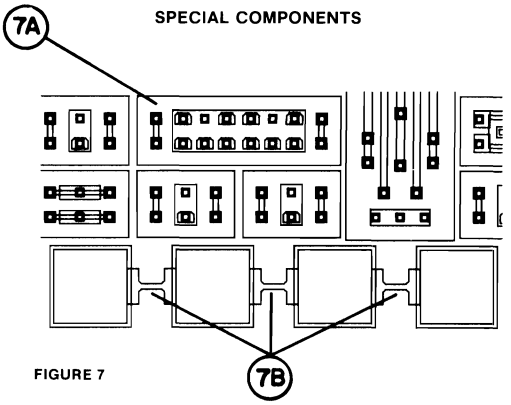


FIGURE 7

DESIGN CONSIDERATIONS

The design of circuit functions for optoelectronic ICs in many cases does not require any special considerations. Two significant exceptions are the photodetector-to-signal processing interface, and the effects of incident light on the circuit (since every transistor is also a small photo-transistor). Figure 8 shows several light measurement circuits applicable to the 3500 array. Each of these techniques is designed to extract photocurrent at a fixed reverse voltage,minimizing the charging and discharging of the detector-capacitance with changes in light level. Photocurrent measurement is usually preferred to photovoltaic, since the current is directly proportional to illumination and linear over 5 orders of magnitude. In addition, a reverse bias reduces the junction capacitance. Note that circuit (B) places the collector substrate diode between a low impedance node and common, out of the measurement loop. Circuits (D) and (E) are designed to operate the detector at zero volts (short circuit current mode). This configuration provides the lowest possible dark current.

PHOTOCURRENT EXTRACTION TECHNIQUES

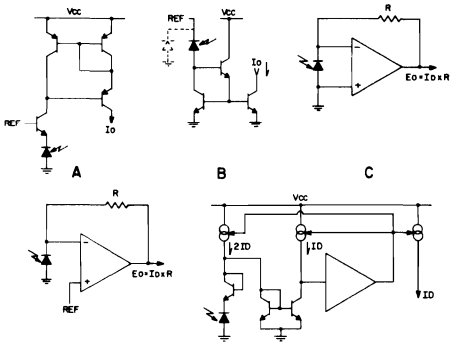


FIGURE 8

With regard to stray photocurrents, this can be a problem for designs where the operating conditions include high values of illumination. The light-induced leakage currents can cause circuit malfunctions, especially at high impedance modes. There are three solutions:

1. Circuit designs that avoid high impedance "off" states at bright light levels.
2. Use of compensating photocurrent sources.
3. Selective masking of the chip to attenuate the illumination impinging all transistors except the detector This can be accomplished by depositing a layer of aluminum above the passivation.

The term "compensating photocurrent source" refers to a transistor added to a circuit for the purpose of providing a light induced current that effectively compensates stray photocurrents. Figure 9 shows a transistor (Q6) added to compensate the light-induced leakage current of Q1, which if uncompensated would tend to turn on Q2 at bright light levels. The advantage of this solution is its negligable impact on the cost of the IC, whereas the metal overcoat approach adds process steps and therefore expense.

STRAY PHOTOCURRENT COMPENSATION

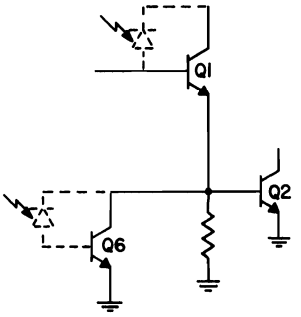


FIGURE 9

9

DESIGN AIDS

To assist in the modeling of optoelectronics circuits for integration using the GENESIS 3500, there are available "breadboard" kit arrays. These include photodetectors and transistors housed on transparent molded packages. These kit arrays permit the modeling of both optical and electrical performance, as well as the effects of stray photocurrents. In addition, there are available packaged functional circuit blocks (macrocells).

PACKAGING & TESTING

The following packages are available for GENESIS 3500 assembly

- 8 Lead DIP outline with integral recessed window.
- 8 Flat Pack.
- 14L and 16L DIP Industry Standard Outlines.

BREADBOARD KIT MACROCELLS

CS-3501

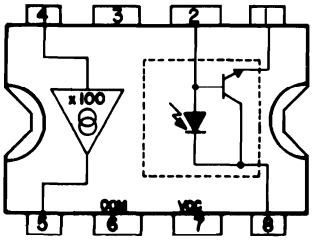
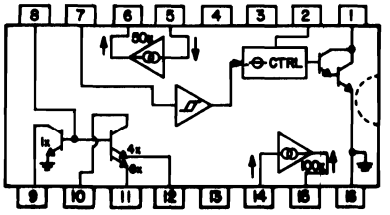


FIGURE 10

CS-3502



All packages are molded transparent epoxy. This packaging capability is fully supported by specialized test apparatus that includes computer controlled light sources at both wafer probe and final test. Figure 11 is a block diagram of the test light source. The lamp is operated at a fixed, regulated current to establish a known color temperature of 2850K. The filter assembly shifts this color temperature input to 4700K. A servo-controlled variable iris regulates the input to an optical integrating sphere. The output of the sphere is coupled to the IC under test and servo control loop via fiber optic cables. Programmable range of the source is 0.1 LUX to 200 LUX.

TEST LIGHT SOURCE

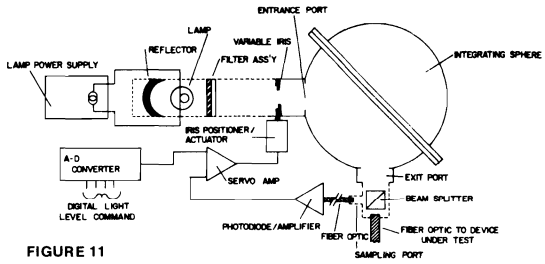
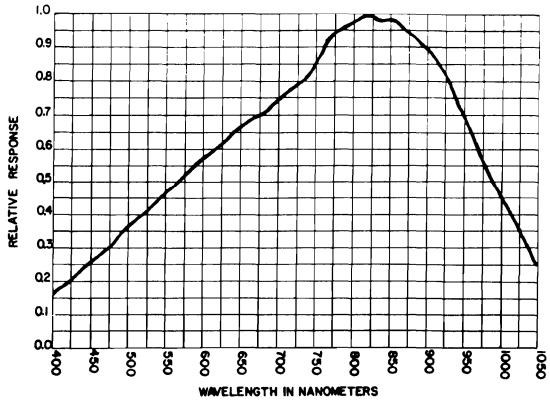


FIGURE 11

PHOTODIODE SPECTRAL RESPONSE CHARACTERISTIC



PHOTODIODE SPECTRAL RESPONSE CHARACTERISTIC.

FIGURE 12

SEMI-CUSTOM OPTOELECTRONICS

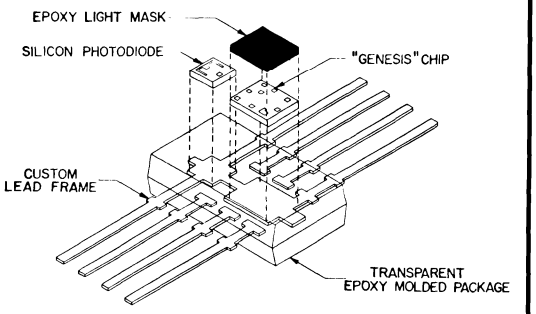
GENESIS™

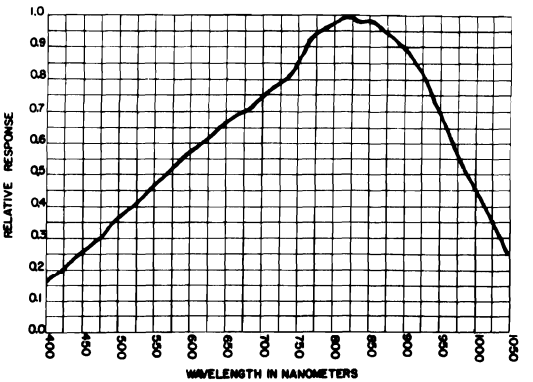
GENESIS light sensitive semi-custom IC's consist of a silicon photodetector combined with a custom designed monolithic chip and housed in a transparent package.

This concept allows optoelectronic functions and systems to be implemented with a single component, often in less space and at a lower cost than an equivalent discrete circuit. Elimination of external photodetector connections reduces errors due to stray leakage paths. The availability of combined photodiode/discretionary masked linear array assemblies has made custom optoelectronic components practical for applications with volume requirements as low as 10,000 pieces.

GENESIS light sensitive IC's are particularly well suited to analog control applications. The photodetectors exhibit good linearity over a photocurrent range of 50 picoamps to 50 microamps.

Currently, two photodetector sizes, three semi-custom "control chip" arrays and two package options are available. The arrays are all bipolar and are customized by adding a unique interconnection pattern to a pre-processed wafer. Each interconnection pattern defines a new custom IC. Both detectors are silicon photodiodes and are identical except for active area. The anode is always connected to the substrate. This allows a mechanically stronger lead frame design and permits the photodetector-to-control chip interconnect to be accomplished with a single internal wire.





PHOTODIODE SPECTRAL RESPONSE CHARACTERISTIC

ARRAYS

DESIGNATION	SIZE (mils)	NPN	PNP	R	BOND PADS	Vcc RANGE
2000E	70 x 70	48	15	124	18	0.7 to 20V
2500G	75 x 79	58 / 2*	18	247	18	"
3000F	90 x 110	92 / 4*	36	305	24	"

* POWER TRANSISTORS

DETECTORS

DESIGNATION	SIZE (mils)	ACTIVE AREA	USABLE SPECTRUM	SENSITIVITY, TYP.		CAPACITANCE	DARK CURRENT
				PHOTOPIC	RADIOMETRIC*	(0V)	(0.6V, +50C)
809	44 x 44	1 mm^2	450-1050 nM	0.7 nA/LUX	4 nA/mW/CM^2	100 pF	2 nA
811	50 x 50	1.5 mm^2	450-1050 nM	1.1 nA/LUX	4 nA/mW/CM^2	150 pF	3 nA

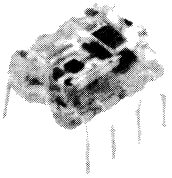
* AT 900 $_N$M

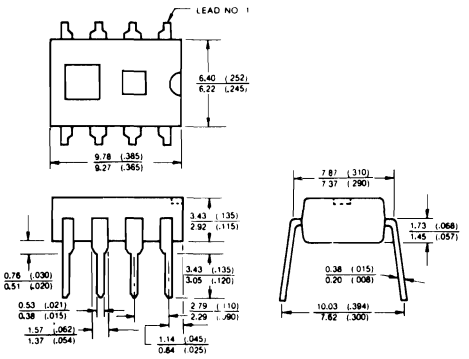
9

The transparent DIP package has the same lead spacing and is approximately the same size as a standard 8 lead "Mini-Dip" A molded-in recess on the top surface is provided directly over the detector This reduces abrasion of the light sensitive surface during handling and also can be used as a filter retainer Pin 5 is internally connected to the detector anode and control chip substrate.

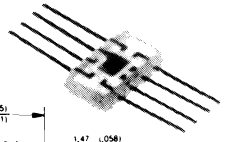
The transparent 8 lead flatpack is ideally suited to applications where minimum size is essential. Pins 1, 5 and 8 are all interconnected internally in order to adequately support the bond pads. Since these leads are committed to the substrate and detector anode connections, pinout is limited to 6 leads.

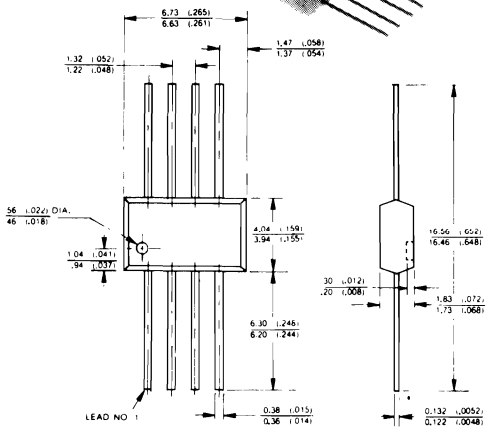
8L DIP





FLATPACK





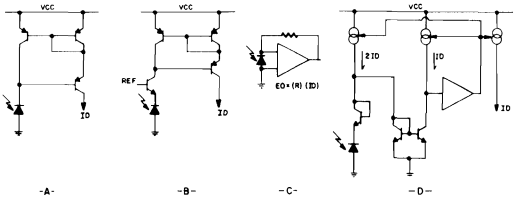
1 PHOTOCURRENT EXTRACTION: Configuration of the photodiode as a current generator provides several orders of magnitude of useful signal, proportional to illumination. Configured as a voltage source, the photodiode output is limited to a narrow range and is non-linear This drawing depicts 4 useful current-mode configurations. All are designed to provide a buffered current source whose value is equal to or a multiple of the detector current.

Circuit 1A is simply a "Wilson" current mirror and is most useful when the supply rail is regulated. Above 5 volts, the detector leakage current will restrict the minimum attainable sensitivity.

Circuit 1B adds an NPN buffer device to allow the detector voltage to be established independent of Vcc.

Circuit 1C utilizes an op amp to operate the detector at zero volts. This provides the lowest dark current and best linearity. Since the output is a voltage, overall dynamic range is reduced, although a diode can be substituted for the feedback resistor to compress the range logarithmically. Linearity at low currents is degraded by the input bias currents of the op amp.

FIGURE 1 PHOTOCURRENT EXTRACTION TECHNIQUES



Circuit 1D provides the widest dynamic range and best linearity possible with an all bipolar circuit. This circuit has been used to extract detector currents over the range of 50pA to 10uA. The detector voltage is within 30mV of zero throughout the range. Disadvantages of this configuration include the necessity of an external compensating capacitor and a slow response time at low light levels.

SHORT CIRCUIT CURRENT EXTRACTOR

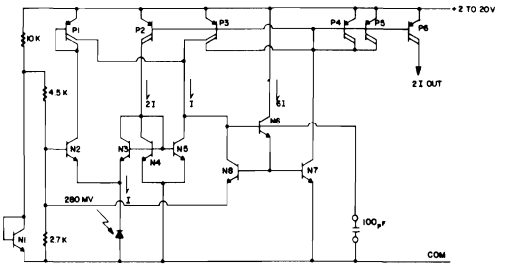


FIGURE 1D

2. This is a realization of Circuit C. When operated from a single +5V supply, this amplifier will output a voltage proportion to illumination with a typical linearity of better than 1% over two decades. Output range is 0 to 3.5V

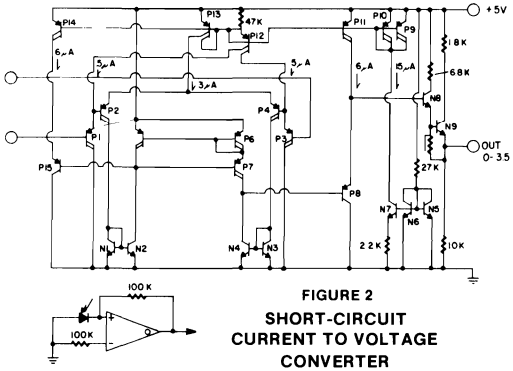


FIGURE 2
SHORT-CIRCUIT CURRENT TO VOLTAGE CONVERTER

3. PROGRAMMABLE PHOTOCURRENT AMPLIFIER: This circuit is ideal for increasing the value of the photocurrent by a fixed multiple. The gain is constant over a wide current range and is temperature independent when programmed with Circuit 4.

PROGRAMMABLE CURRENT GAIN CELL

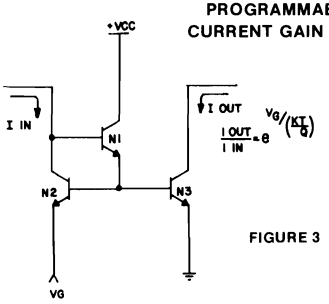


FIGURE 3

4. PROGRAM VOLTAGE SOURCE: N3 and N4 are operated at half the emitter current density of N2, to establish a ΔVBE of approximately 18mV at 25C. The R2/R1 ratio is used to raise the voltage to the desired level. Q1 is used as a start-up device.

GAIN PROGRAMMING VOLTAGE SOURCE

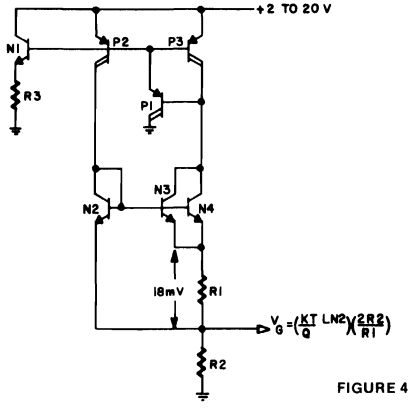


FIGURE 4

5. COMPLETE AMPLIFIER: Combines Circuits 3 and 4. Note that the "KT/Q" terms cancel and that the gain is established by emitter current and resistor ratios. Useful gain range is 1 to 200. Above 200, base current errors cause the gain to be lower than the programmed value.

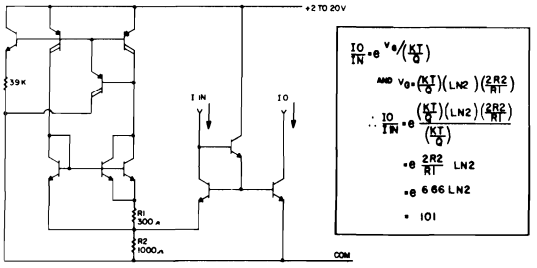


FIGURE 5

6. AMPLIFIER WITH SELECTED GAIN: By switching in-and-out additional transistors, the gain can be selected remotely. In this example, the added NPN provides additional gain to establish a hysteresis loop. When the photocurrent exceeds a threshold value, it is abruptly increased to ensure a positive switching action.

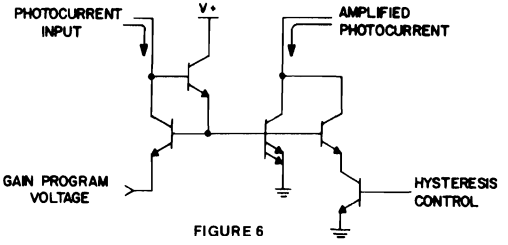


FIGURE 6

7. COMPARATOR: If the amplified photocurrent is returned to the supply rail through an external resistor, a light dependent voltage is established. To provide a load switching function at a programmed light level, a voltage comparator can be used. This simple comparator configuration has a common mode input range from zero to Vcc-1.8V and provides voltage hysteresis to ensure positive switching action.

COMPARATOR WITH HYSTERESIS

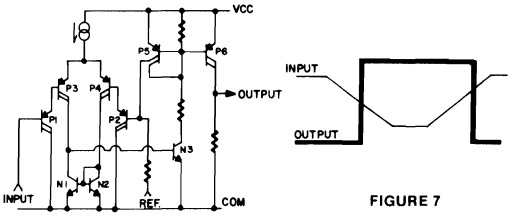


FIGURE 7

9

8, 9. A COMPLETE OPTOELECTRONIC SYSTEM: This circuit has been fabricated using the CS-2500 and 811 Detector It is a general purpose optoeletronic system that can be configured for multiple applications. The individual blocks are described below.

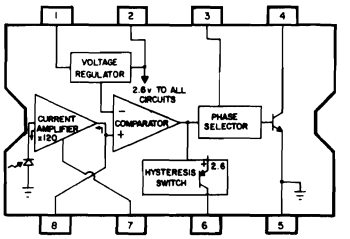
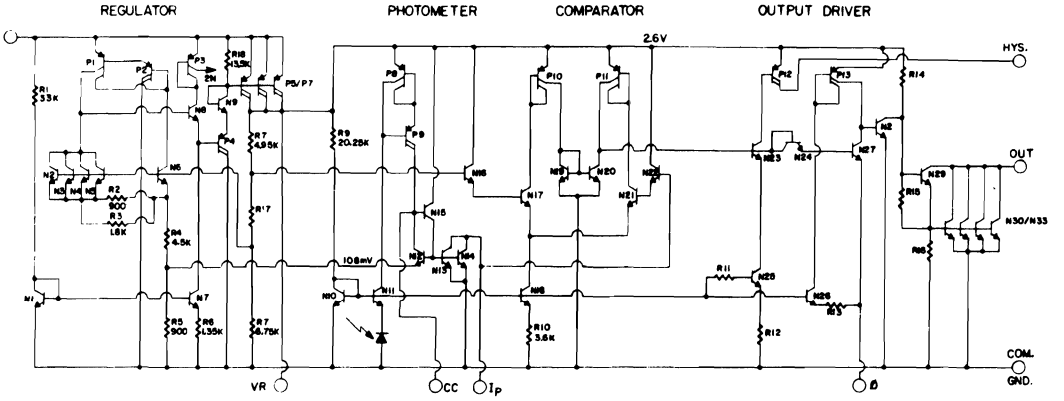


FIGURE 8

FIGURE 9



10. PHOTOMETER: Consists of a variation of photocurrent Extractor 1B and a programmed current amplifier.

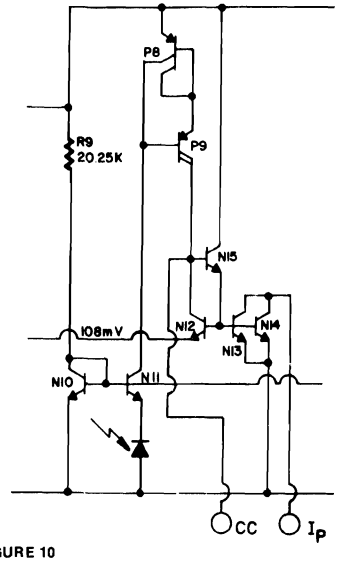


FIGURE 10

11 COMPARATOR: The use of Darlington NPN input stage provides very low input bias currents.

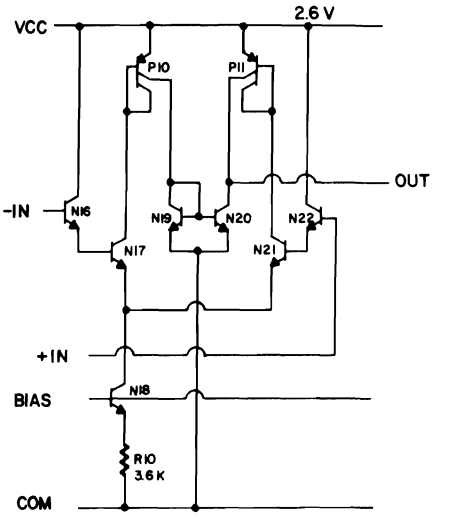


FIGURE 11

12. OUTPUT DRIVER and HYSTERESIS SWITCH: Connection of the phase (ϕ) pin to common or V_R programs the input-to-output phase relationship of the driver For light-sensitive-switch applications, this permits configuration as a "normally on" or "normally off" function. N23 and P12 provide an output that can be used to apply positive feedback (hysteresis) to the input of the comparator.

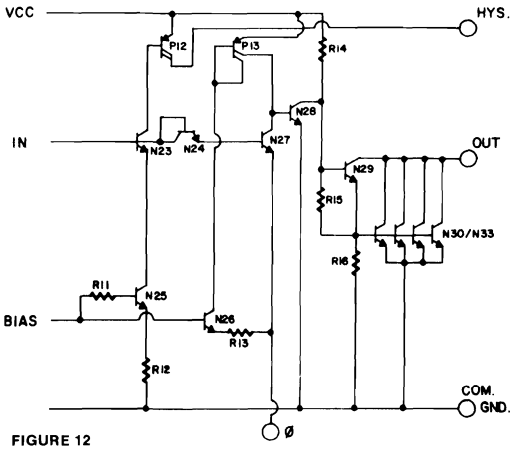


FIGURE 12

13. REGULATOR: Establishes a regulated 2.6V rail to operate the photometer and comparator This circuit also provides a voltage reference for the comparator and the photocurrent amplifier program voltage.

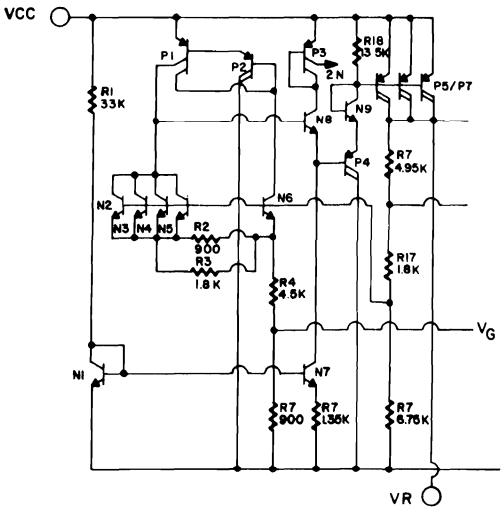
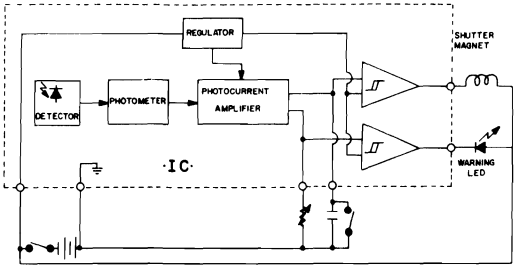
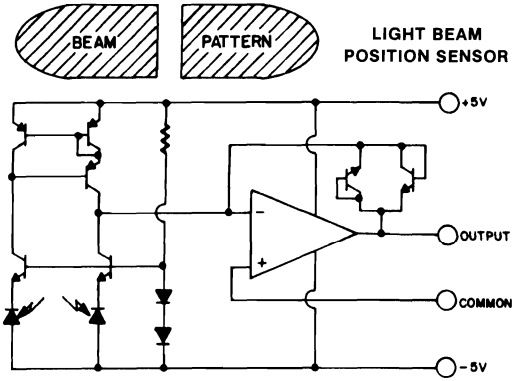


FIGURE 13

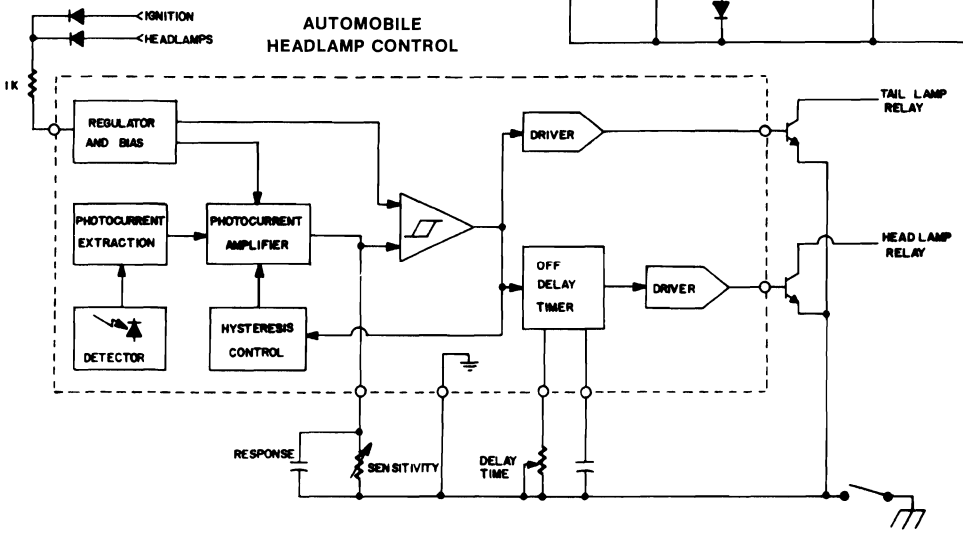
CAMERA EXPOSURE CONTROL



LIGHT BEAM POSITION SENSOR



AUTOMOBILE HEADLAMP CONTROL



9

QUESTIONS and ANSWERS
GENESIS™ SEMICUSTOM ICs

MANUFACTURING

Q. Where are GENESIS ICs manufactured? Does CSC™ process their own wafers?

A. All *GENESIS* wafers are fabricated in our East Greenwich, RI facility. Packaging is sourced at several locations.

Q. Can CSC handle high volume production requirements?

A. We routinely ship in excess of one hundred thousand devices per month of a single *GENESIS* IC type. An inventory of several thousand pre-processed *GENESIS* wafers assures a rapid ramp-up to high volumes.

Q. If my production requirements increase, can CSC manufacture a "full custom" version of my IC? What expense is involved?

A. Since much of our business is full custom and application specific ICs, we are fully staffed and equipped to convert your *GENESIS* design to a higher level of integration. This generally involves a dedicated CAD layout and generation of a complete set of photomasks. The cost depends on chip size, and is typically in the range of $15,000 to $30,000.

Q. Can GENESIS ICs be multiple sourced?

A. In most cases, yes, since the arrays of other semicustom manufacturers are topographically similar to ours. You would contract integration of your IC separately with each vendor, as the interconnect mask of one supplier will not align with the pre-processed wafers of another, even when the topography appears identical.

A disadvantage of multiple sourcing is higher unit pricing, since each vendor only produces part of the total production volume. Additionally, the cost of artwork, photomasks, prototypes and test programs are incurred more than once.

Q. If my IC is single sourced by CSC, how can I be assured of continued delivery?

A. CSC has instituted a number of steps that may preclude the need for multiple sourcing:

1. We maintain an uncommited pre-processed wafer inventory of several thousand wafers.
2. An alternate source has been qualified to manufacture *GENESIS* wafers, should the need arise.
3. Database copies of all CAD layout files are maintained at a remote location.
4. The original photomask reticles are stored at another remote site.
5. Packaging is multiple sourced.
6. CSC, will at your request, and based on a firm scheduled delivery commitment, produce an inventory of finished wafers and/or packaged ICs.

DESIGN and INTEGRATION

Q. What services are included in your "integration"?

A. Assuming that you provide a circuit schematic and layout, CSC performs the following steps:

1. Our engineers will review the design for potential problems.
2. Your circuit and layout are cross checked for accuracy.
3. The layout coordinates are entered (digitized) into our CAD system.
4. A second schematic to layout verification check is performed.
5. A design rule check program is run to ensure compliance.
6. The data is converted to pattern generator format and output on magnetic tape.
7. The dedicated level photomask(s) is fabricated.
8. A wafer is processed using the custom photomask(s).
9. The wafer is diced, prototypes are assembled in ceramic DIL packages and functionally tested.

Q. How many prototypes are included?

A. You may select either 20 functionally tested or 40 untested prototypes. If the functional test requires other than DC measurements, you must supply us with a functional test apparatus.

Q. Can we purchase additional prototypes?

A. Yes. Price, minimum quantity and delivery can be quoted on an individual basis.

Is there an additional charge for test programs?
The cost of production test program generation is included in our integration charge. But we do not proceed to tually write the program until the prototypes have been approved and we have a delivery release for production quantities.

What do you define as "production quantities"?
A minimum of 10,000 ICs deliverable over one year.

Does CSC require a production volume purchase commitment?
Both IC integration and layout are available as "stand alone" services, with no further commitments required.

Do you offer design services?
IC circuit design service is available directly from CSC to customers with a minimum production requirement of 100,000 ces per year. IC design is a "bundled" service, available only combined with layout and integration.

What is the typical design charge for a GENESIS IC?
$15,000 to $25,000.

What does it cost to make a change to my IC?
The integration charge for a design iteration is 50% of the original cost. The charge for relayout service depends percentage of the circuit impacted:
<33% impacted..... 50% of applicable layout charge.
>33% impacted.....100% of applicable layout charge.
layout charge does not apply if you do the modifications yourself on a *GENESIS* layout sheet.

I am not prepared to design my own IC, but my production requirements are small. What options do I have?
CSC can recommend independant contractors that offer IC circuit design on a fee for service basis. We have designated ecific vendors as "***GENESIS* Authorized Design Consultants**". These sources have been qualified by us regarding ir semicustom IC design capability, and have direct access to our design tools and engineering staff.

How proprietary is my IC?
CSC guarantees not to sell your *GENESIS* IC to a third party, or integrate a direct copy, without your written consent. further agree not to divulge any details of the IC to others without your permission, unless this information is already he public domain. To discourage another party from copying your chip, we automatically register the dedicated photomask ttern(s) with the United States Copyright Office, under the Semiconductor Chip Protection Act, at no expense to you.

What is the delivery time for GENESIS prototype integration?
If you supply us with a circuit schematic and completed layout sheet, lead time to prototypes is 6 to 8 weeks for ear chips and 10 to 12 weeks for digital integrations. If CSC performs the IC layout, allow an additional 2 weeks.

What is the production lead time after approval of samples?
For linear ICs in standard dual-in-line plastic packages, 8 weeks to first delivery. Digital ICs and other package styles quire up to 3 additional weeks.

ST and QC

Are production ICs tested 100%, or on a sample basis?
All packaged *GENESIS* production ICs are tested 100% both at the wafer level and as a finished assembly, at +20C. addition, a sample from every lot shipped is subjected to further testing as part of our standard outgoing QC procedure. packaged ICs (dice) are 100% electrically tested at wafer probe, 100% visually inspected after sawing, and sample pected at outgoing QC.

Are there any standard outgoing quality criteria for GENESIS ICs?
All outgoing lots are inspected to MIL-STD 105D, single sampling plan. Our standard lot acceptance levels is 0.065% ctrical parametric AQL. The parametric AQL applies to all test parameters supported by a worst case analysis (3 ma limits) supplied by the designer of the IC.

Is 100% burn-in available?
Yes, at extra cost. Both static and dynamic burn-in are available. There is a non-recurring tooling charge to design d build the burn-in boards. The amount depends on the burn-in cycle, test circuit complexity and the quantity of s to be shipped per month. Longer burn-in times increase the number of board positions required to support a given p level. We usually recommend a 24 hour, +135C cycle. There is normally an additional 100% electrical test after rn-in.

Is testing available at temperatures other than +20C?
Yes. CSC has the capability to provide 100% testing at temperatures from -55C to +150C, at extra cost.

QUOTATIONS and GENESIS ONLINE™ SYSTEM

Q. What information is required to obtain tooling charge and unit price estimates?

A. 1. The ***GENESIS*** chip to be quoted.
2. Approximate number of NPN and PNP transistors in your circuit.
3. Package style and number of pins.
4. Quantity requirements.

Q. How do I actually obtain the quote or estimate?

A. CSC provides a number of options for convenient, fast and accurate response:

1. Phone our nearest representative with the details listed in the previous question. Response is normally provided within 1 working day. CSC has sales representatives throughout the U.S.A., and in selected locations in Europe and the far east.
2. Phone the factory directly (*GENESIS* sales). Verbal response is often provided the same day, with a follow up letter or telex.
3. For an **instant quote**, phone the ***GENESIS onLine™*** technical bulletin board system. This service is available 24 hours a day*, 7 days a week, exclusively for use of our customers. To access this system, you must first register and obtain a password; there is no cost or obligation.
   *Except for system maintenance periods, 4 to 8 hours per week.

Q. What exactly is the GENESIS onLine™ technical bulletin board system?

A. A telephone-accessible computer database located in our factory. You are automatically connected to the computer when you reach the ***GENESIS onLine™*** phone number.

Q. What services are available?

A. 1. ***GENESIS onLine™* Quote** . . . instant quotations for production pricing, integration charge, and layout service.
2. ***GENESIS*** design library CAD downloads. These are files that can be electonically transferred from our computer to yours. Included are SPICE© and PSPICE© models for the ***GENESIS*** IC components, and netlists for the pre-designed circuits in the design library. These files are regularly updated and expanded.
3. Message board . . . where you can leave inquiries for our engineers, obtain additional information, order breadboard arrays, etc.

The Technical Bulletin Board System is provided as a service for the exclusive use of registered qualified engineers, buyers, and our customers.

Q. How do I access this service?

A. First you must register with us (contact either our local representative or sales department), and receive a log on password. We will need to know what type of computer you are intending to use so that we can format the data properly for your terminal. Access to this system is controlled and limited for two reasons: to maximize the availability of the system, and to exclude "hackers" (and competitors). You will be given the dedicated phone number, and a short manual describing how to use the system.

Q. What hardware do I need?

A. ***GENESIS onLine™*** supports IBM compatible computers. In addition to the PC, you will need either a 300 BPS or 1200 BPS modem and a terminal emulation software package.

While the TeleQuote program can be operated from most terminals, the PSPICE© netlists will probably only be useful to those with MS/DOS© computers.

Q. What is the GENESIS onLine™ character transmission protocol?

A. Full duplex. 10 bit characters, consisting of 1 start bit, 8 data bits, and 1 stop bit; no parity. We also support the CP/M XMODEM protocol for error-free downloads. This option can be selected while online.

Q. How long is an "onLine" quotation valid? Are there any other stipulations?

A. The quotation is valid for 30 days and the following stipulations apply:

1. The *GENESIS* chip, component utilization, package style and package size are as specified.
2. The resistance requirements of the circuit are within the physical layout constraints of the chip selected.
3. All test parameters are attainable on a worst-case basis; designer must supply supporting computations.
4. Only DC tests at 20C will be performed; up to 2 tests per device pin.

Experience & Capabilities

Since its beginning in 1972, Cherry Semiconductor has maintained a strong commitment to excellence in the design and manufacture of bipolar integrated circuits. Over the years CSC has expanded and is now a major supplier of custom bipolar ICs for Automotive, Memory Management (Computer Peripherals), Power Supply and Motor Control applications.

Processing technologies include Linear Bipolar, I^2L Digital, Linear I^2L combinations on the same chip, Optoelectronic Circuits, Low Power Schottky and Flip-Chip Metallurgy.

CSC has the design engineering expertise to take a custom circuit from concept to finished product. A full array of design tools is employed to ensure that the final product meets all customer requirements. These include worst-case circuit analysis utilizing the PSPICE computer aided circuit simulation program, complete CAD facilities for interactive color-graphic circuit layout and pattern generation, and in-depth statistical process control.

Our modern plant has been furnished with the latest processing and production equipment, including microprocessor controlled diffusion furnaces, projection mask aligners, vertical epitaxial reactors, electron beam evaporators, sputtering systems, scanning electron microscope (SEM), and computerized testing stations. All critical processing steps are performed in a VLS I environment in Class 100 clean rooms, specially controlled for temperature and humidity, and isolated from external vibration.

Of equal importance to our extensive experience and modern manufacturing facilities, is our approach to the custom circuit business. CSC is open and straightforward with its recommendations. We do a lot of pre-quotation engineering in order to properly define the requirements of a program, and we make sure that a correct "match" exists, both technically and economically.

Choosing A Custom Circuit

A full custom circuit is chosen for specific reasons, and usually when substantial production runs are expected. While engineering and tooling costs are a one-time charge, they can be substantial. It is to the users benefit that these costs be amortized over a large piece-part base. Where large quantity requirements exist, engineering charges become relatively insignificant, and low unit prices are realized. Custom circuits can be very cost-effective in combining diverse and/or proprietary circuit functions, and in the replacement of several discrete packaged functions with a single circuit. Even in applications where only moderate production runs are anticipated, a custom circuit can sometimes be justified by the reduction in board space, handling and inventory costs. Each situation must be considered on its own merits. Some of the more important considerations are itemized in the following list of "advantages" and "disadvantages".

Advantages

1. *Proprietary Design:* Unique circuit functions and combinations can be incorporated in a single chip.
2. *Lower Costs:* By combining many functions on a single chip, assembly, test, handling, and inventory costs are all reduced, compared to separate discrete components.
3. *Space Savings:* Significant reductions in printed circuit area are usually obtained. In many applications this can be of singular importance.
4. *Higher Reliability:* By reducing the number of individual circuits and connections there is a demonstrable improvement in overall system reliability.

Disadvantages

1. *Long Lead Time:* 20 to 27 weeks to prototypes and 32-50 weeks to production is typical. Actual lead time depends on several factors such as circuit complexity.
2. *Engineering & Tooling Costs:* One time charge for design, layout, test programs and initial samples. Costs vary, but normally are justified only by large volume requirements.
3. *Modifications:* Possible need to modify if first samples do not perform to exact specifications, resulting in extension of lead time.

Processes Available

CSC processing technology is devoted exclusively to Bipolar, including Linear and Linear Compatible I²L Digital. A number of individual processes and process options are available, and are chosen for the particular application. Maximum operating voltage is usually a prime consideration, and CSC includes processes which cover a range from 6 volts to as high as 60 volts.

In addition to the (7) "standard" processes available in Linear and Linear/I²L, CSC offers a special 14V process which features a 1.5 micron shallow base diffusion for higher density, higher frequency applications.

These processes are briefly summarized on the following charts:

PROCESSES		
VOLTS	SPEC. NO.	DESCRIPTION
ANALOG LSI BIPOLAR (400MHZ) (ALL 3μM BASE DEPTH)		
12	200-003	LINEAR/I²L
17	200-017	LINEAR/I²L
20	200-012	LINEAR
30	200-009	LINEAR
40	200-013	LINEAR
50	200-014	LINEAR
60	200-010	LINEAR
ANALOG/DIGITAL LSI BIPOLAR (1GHZ) (THIN EPI, SHALLOW BASE 1.5μM, HIGH DENSITY)		
14	200-016	LINEAR/LOW POWER SCHOTTKY/DUAL LAYER METAL
ANALOG/DIGITAL LSI BIPOLAR (2.5GHZ) (VERY SHALLOW BASE X, = 0.75μM VERY HIGH DENSITY)		
12	200-021	LINEAR/SCHOTTKY/ECL DUAL LAYER METAL

PROCESS OPTIONS

- DEEP N+ (SINKER, PLUG, WELL) FOR I²L AND POWER TRANSISTORS
- ION IMPLANTED RESISTORS 1, 2, AND 5 KILOHMS/SQUARE
- OXIDE AND NITRIDE CAPACITORS
- LPCVD NITRIDE PASSIVATION UNDER METAL
- SILICON DIOXIDE OR PLASMA NITRIDE FINAL PASSIVATION OVER METAL
- ALUMINUM ALLOYS: Al, Al Cu, Al Si Cu
- ALUMINUM OR PLATINUM SILICIDE SCHOTTKY DIODES
- FLIP-CHIP METALLURGY

Package Options

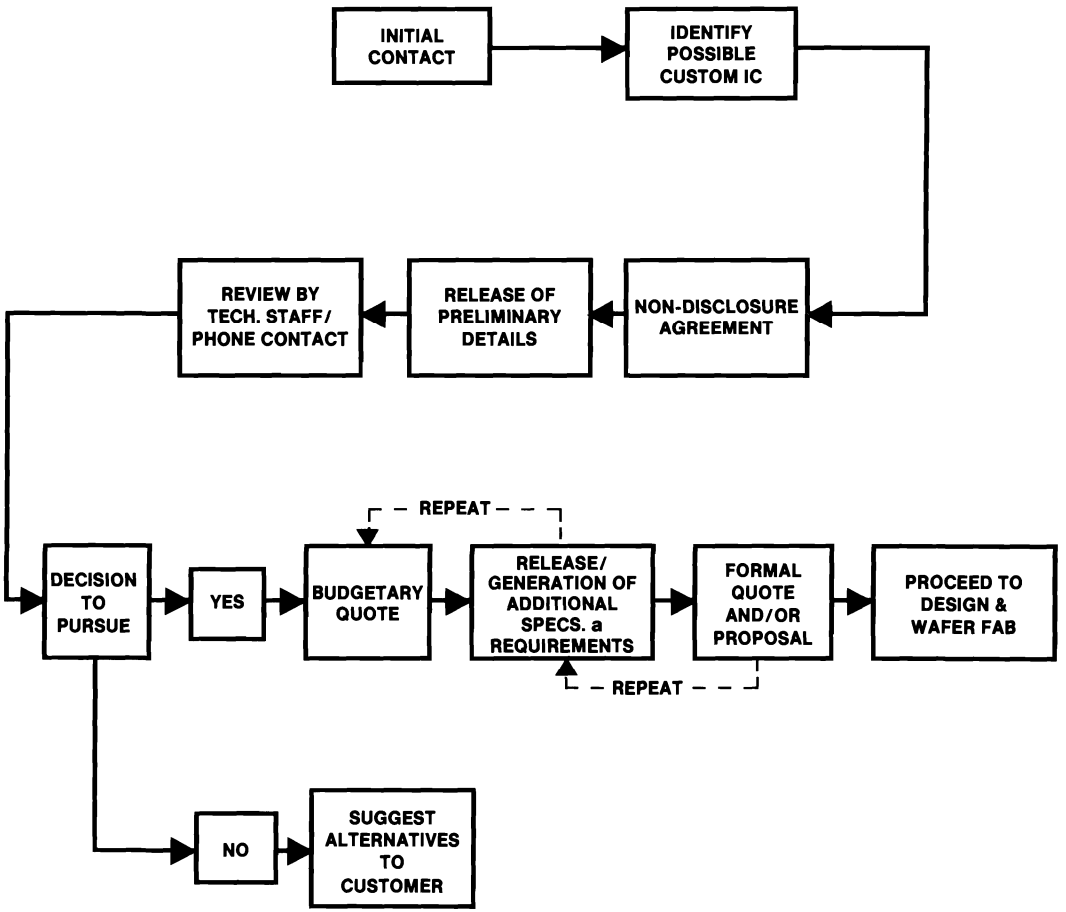
Cherry Semiconductor has a wide range of standard package options that will satisfy a variety of die sizes and circuit applications. Included are conventional dual-in-line plastic and ceramic packages, and 5-lead, 11-lead and 15-lead MULTIWATT® package for power applications. Plastic chip carriers, small outline packages, and flip-chips are available for reflow solder hybrid applications. CSC can also provide other package configurations on a custom tooling basis. Presently available standard types are listed below.

Custom Products Package Availability

* **DIP PLASTIC and CERAMIC (CERDIP)** 8, 14, 16, 18, 20, 22, 24, 28, 40 & 48 Leads
* **POWER PACKAGE** 5 Lead TO 220; 11 and 15 Lead MULTIWATT®; 20 and 24 Lead SO; 16 Lead DIP
* **SO PACKAGE** 8, 14, and 16 Leads Narrow Body, 16, 18, 20, 24 and 28 Leads Wide Body
* **PLASTIC CHIP CARRIERS** 20, 28, 44, and 68 leads
* **TO-92**

Initial contact can be made by the customer, a CSC regional sales manager, or one of our sales representative firms. If a possible custom IC is identified, CSC will issue a non-disclosure agreement to protect the customer's interests. At this point, the customer normally provides more complete information for review by CSC engineering. If a custom IC is technically feasible, and appears to be cost-effective, a decision to pursue is then mutally agreed on. A budgetary quote is then provided by CSC following a more complete review and/or the generation of additional specifications, if necessary. Finally, a formal quote and detailed proposal is made by CSC. If accepted, we will then proceed directly to design & fabrication. A typical program is outlined in the following chart.

Typical Customer Interface



TYPICAL PROGRAM

TASK-MILESTONE	ELAPSED TIME (WEEKS)
★ PROPOSAL PREPARATION	1-2
★ CKT DESIGN, WORST CASE ANALYSIS, BREADBOARD CONSTRUCTION AND DELIVERY TO CUSTOMER	4-6
★ CUSTOMER BREADBOARD EVALUATION	1
★ PREPARE LAYOUT SPEC	1-2
★ TOPOLOGICAL LAYOUT	8
TEST PROGRAM GENERATION	
★ MASKS	1
★ WAFER FAB	3-5
★ CIRCUIT PROBE, ASSEMBLE, TEST	1-2
DELIVER ENGINEERING SAMPLES	*20-27*
★ OFFSHORE ASSEMBLY	2-5
DELIVER QUALIFICATION SAMPLES	
★ DEVICE CHARACTERIZATION	1-3
★ PROBE STATION EVALUATION	1-3
★ QUALIFICATION TESTING	8-12
RELEASE TO PRODUCTION	
TOTAL ELAPSED TIME:	*32-50 WEEKS*

CHERRY SEMICONDUCTOR CORPORATION 2000 South County Trail, East Greenwich, R.I. 02818
(401) 885-3600 FAX: (401) 885-5786 Telex: WUI6817157